Texas Instruments

TMS320DM320 Imaging Peripherals Vol - 3

Technical Reference Manual Version 1.0

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1 CCD Controller

The CCD Controller captures and processes the raw data from the CCD sensor. The A/D converter and Timing Generator for CCD sensor are external to DM320 chip. The functions of CCD controller are output formatting, digital clamping, gain and offset control and decimation for physical image capturing.

1.1 Features

Generates timing signals VSYNC / HSYNC and field ID

Can synchronize to externally provided VSYNC / HSYNC signals

Supports progressive scan and interlaced CCD

Generates optical black clamping control signals

Programmable culling pattern

Maximal supported pixel clock is 100 MHz

Maximal supported CCD imager size 4096 X 4096

Digital clamping

Black level compensation

Median filtering

Gain and offset control

10-bit to 8-bit A-law compression

Supports CCIR601/656 Digital YCbCr 4:2:2 (8/16bit) interface

Supports Bayer and Foveon input data format

Supports VGA read out mode

Supports up to 14-bit analog front end

Supports various image data format like Sony, Matsushita etc

Refer Figure 1 for details about CCDC processing blocks.

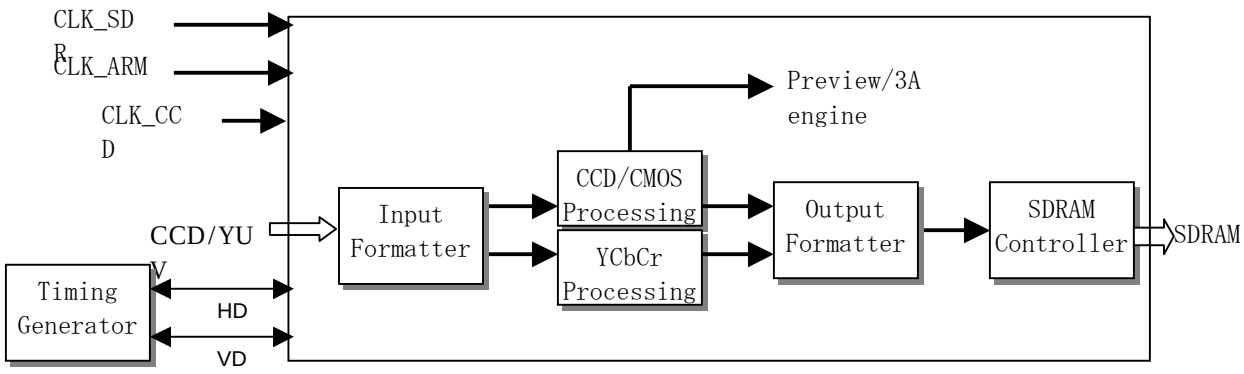


Figure 1: CCD Controller Block Diagram

1.2 CCDC Input Signal Interface

Timing and control of the interface is done using the HD, VD, field ID, pixel clock, and write enable signal. The CCD Controller accepts pixel data via the CI7-CI0,YI7-YI0 input pins. The definition of each pixel input is determined by the input format selected in the input formatter. The definition for signals in each mode is shown in Table 1. The interface consists of a set of signals used to transfer raw CCD data from an imager to the CCD Controller. Additionally, the CCD controller can be configured to operate in a mode that adheres to the CCIR 601/656 interface specification. The CCIR 601/656 specification provides a standard method, to transfer 8/16-bit, YCbCr-4:2:2 formatted video data. The pixel clock clocks data into the CCDC at a maximum rate of 100 MHz. When the CCDC is configured to write data to SDRAM, raw CCD data will be written to SDRAM. Details of the interface are given in Table 2.

Pin Name	CCD	16-bit YCbCr	8-bit YCbCr
CI7		Cb7,Cr7	Y7,Cb7,Cr7
CI6		Cb6,Cr6	Y6,Cb6,Cr6
CI5	C_DATA13	Cb5,Cr5	Y5,Cb5,Cr5
CI4	C_DATA12	Cb4,Cr4	Y4,Cb4,Cr4
CI3	C_DATA11	Cb3,Cr3	Y3,Cb3,Cr3
CI2	C_DATA10	Cb2,Cr2	Y2,Cb2,Cr2
CI1	C_DATA9	Cb1,Cr1	Y1,Cb1,Cr1
CI0	C_DATA8	Cb0,Cr0	Y0,Cb0,Cr0
YI7	C_DATA7	Y7	Y7,Cb7,Cr7
YI6	C_DATA6	Y6	Y6,Cb6,Cr6
YI5	C_DATA5	Y5	Y5,Cb5,Cr5
YI4	C_DATA4	Y4	Y4,Cb4,Cr4
YI3	C_DATA3	Y3	Y3,Cb3,Cr3
YI2	C_DATA2	Y2	Y2,Cb2,Cr2
YI1	C_DATA1	Y1	Y1,Cb1,Cr1
YI0	C_DATA0	Y0	Y0,Cb0,Cr0

Table 1: CCDC Data Input Formats

The CCDC supports 8 to 14-bit wide raw data signals. When the CCD has fewer than 14 data lines, connect the un-used data lines to ground.

CCDC input mode is selected using field IMPMOD in register *MODESET*

Name	I/O	Function
C_DATA[13]-C_DATA[0]	I	Raw Image data loaded by CCD. Bit width can be can be configured to 8 to 14 bits. The polarity of the input image data can be reversed.
C_VSYNC (VD)	I/O	VSYNC. Vertical synch signal. This signal can be configured as an input or an output. When configured as an input, the external CCD or CMOS sensor must supply the VD signal. When configured as an output the DM320 will supply the VD signal. The polarity of VD can be reversed.
C_HSYNC (HD)	I/O	HSYNC. Horizontal synch signal. This signal can be configured as an input or an output. When configured as an input, the external CCD or CMOS sensor must supply the HD signal. When configured as an output the DM320 will supply the HD signal. The polarity of HD can be reversed.
C_FIELD	I/O	Field identification signal. This signal can be configured as an input or an output. When configured as an input, the external CCD or CMOS sensor must supply the field identification signal. When configured as an output the DM320 will supply the field identification signal. When the field identification signal is set to be an input to the DM320, this signal can be configured to be latched by the VD signal. The polarity of the field identification signal can be reversed.
C_PCLK	I	Pixel clock. This signal is the pixel clock used to load image data into the CCDC. The Clock controller can configure to trigger on the rising or falling edge of the PCLK signal. The maximum pixel clock rate is 100MHz.

Table 2: CCDC Signal Interface

1.3 Frame Setup

ARM controls width, polarity, position and direction of internally generated signals. Figure 2 shows various CCDC register settings related to the frame setup. The shaded area is the physical imager size and the gray area is the valid data area. The image data in this valid data area will be processed and stored to external SDRAM. The vertical start position for even and odd fields can be configured independently. Various registers involved in the frame setup are described in Table 3.

The timing generator provides the use of external sync signals (HD/VD) or internally generated timing signals. The horizontal sampling start point is set in SPH register by using pixel number.

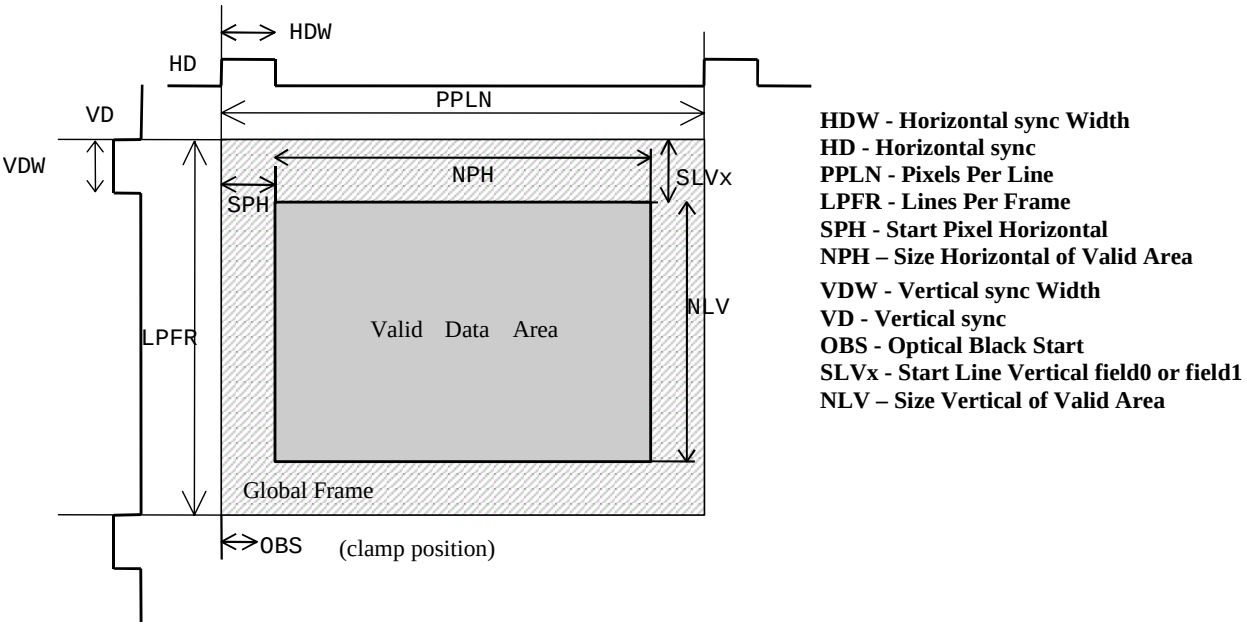


Figure 2 Frame setup

Register	Description
HDWIDTH	HSYNC pulse width
VDWIDTH	VSYNC pulse width
PPLN	Pixels per line
LPFR	Lines per frame
SPH	Start pixel horizontal
NPH	Number of pixels horizontal
SLV0	Start line vertical - field 0
SLV1	Start line vertical - field 1
NLV	Number of lines vertical

Table 3: Frame Setup Registers

All the above registers are latched by VD (see section 1.9)

1.4 CCDC Processing

As shown in Figure 3, the CCDC consists of several data processing modules that format and enhance raw CCD data. There are three destinations for the processed output data, SDRAM, H3A Engine and/or Preview Engine. The important functions of CCDC are given below:

Digital clamping

Data formatter

Black level compensation

Median Filtering

Gain and Offset control

A-Law compression

Output Formatter

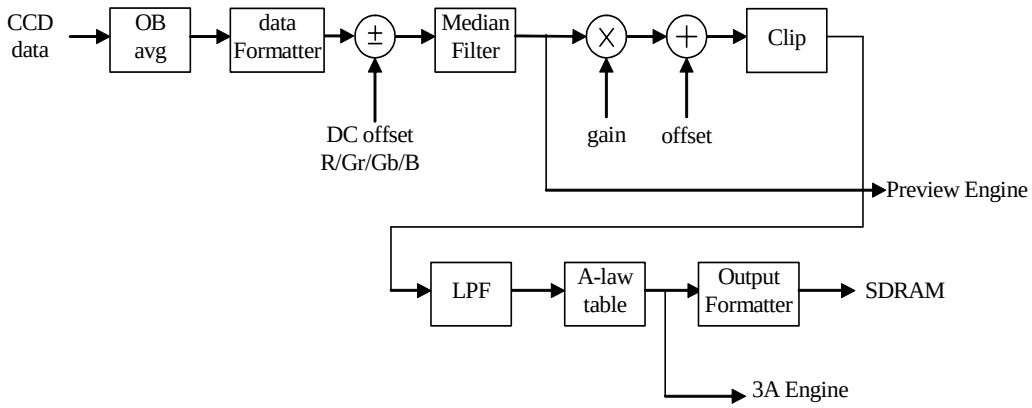
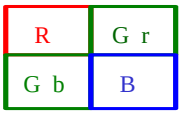


Figure 3: CCD Raw data Processing blocks

1.4.1 Arrangement of CCD Raw Data

CCD controller can accept RGB raw data or complementary color raw data. The color pattern can be decided by the user using register *COLPTN*. The CCDC supports various sensors like Bayer, Foveon etc.



Bayer format with R/Gr and Gb/B in alternate lines – ***Horizontal distance between same colors is 2***

Foveon sensor with R, G, and B in same line – ***Horizontal distance between same colors is 3***

Figure 4: CCDC Color Patterns

1.4.2 Digital Clamp

The first module is the digital clamp block. The image data is latched at the rising or falling edge of the input pixel clock (PCLK). The averaging circuit takes an average of masked (black) pixel values from the image sensor and this value is subtracted from the image data. The user can control the position of the black pixels, the number of pixels (8 or 16) in each line averaged, and the number of lines (8 or 16) averaged.

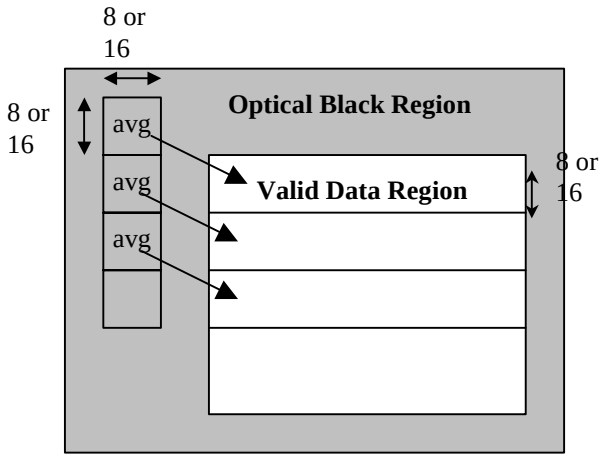


Figure 5: Digital Clamp Block Diagram

Alternately, the user can disable black clamp averaging and select a constant black value for subtraction, instead of using the calculated average value. CLAMP register is used to control the enable/disable and various parameters of clamping and DCSUB register is used to set the DC level to be subtracted from the CCD data.

1.4.3 Black Level Compensation

After the Digital Clamp is applied to the data, Black Level Compensation is applied to the R/Ye, Gr/Cy, Gb/G, and B/Mg signals. The offset applied to the current data sample is selected according to the even/odd phase and the color specified for each phase. Different black level compensation values can be set in the registers *BLKCMP0* and *BLKCMP1.*

1.4.4 Median Filter

The Median Filter‘s threshold is configurable and the Median Filter can be enabled or disabled. The threshold value for the median filter can be set in the register MEDFILT.

1.4.5 Gain, Offset, Clip and Low Pass Filter

A gain factor from 0 to 7.9921875 can be applied to the output of the Median Filter. After multiplying the data by the gain factor an offset can be added to the result. The offset can range from 0 to 1023. The resultant CCD data from gain control is clipped to signed 15bit data, and finally clipped to unsigned 14bit data after offset control.

The low-pass filter consists of a simple three-tap (¼, ½, ¼) filter. The low pass filter on/off can be set by bit LPF of MODESET register.

Different gains and offset can be set by registers RYE GAIN,GRCY GAIN,GBG GAIN,BMG GAIN , OFFSET. The output clipping value for the final stage of CCD processing is set by OUTCLIP register.

1.4.6 A-Law

A-Law function can be used to compress CCD data to reduce storage requirements in SDRAM.

When A-Law table compression is used, 10-bit data can be stored in SDRAM as 8-bit packed data, thus reducing SDRAM storage space requirement by 50% The control of compression by A-law is set by register GAMMAWD.

Note: 10-bit raw data requires 16-bit space in SDRAM for storage.

1.4.6.1 Decimation

The final stage in CCDC raw data processing is a programmable decimation function along the horizontal and vertical directions.

Two registers control the horizontal and vertical decimation of CCD Data. The CULH register sets the horizontal culling for even and odd lines. The CULV register sets the culling along the vertical direction. The LSB of CULV represents the top (0^{th}) line of the CCD, the MSB is the 7^{th} line.

Figure 6 below is an example showing how CULH and CULV apply a decimation pattern to the data. The pixels colored in red are read out to SDRAM.

In this case CULH = 0x59C4 and CULV = 0x0066

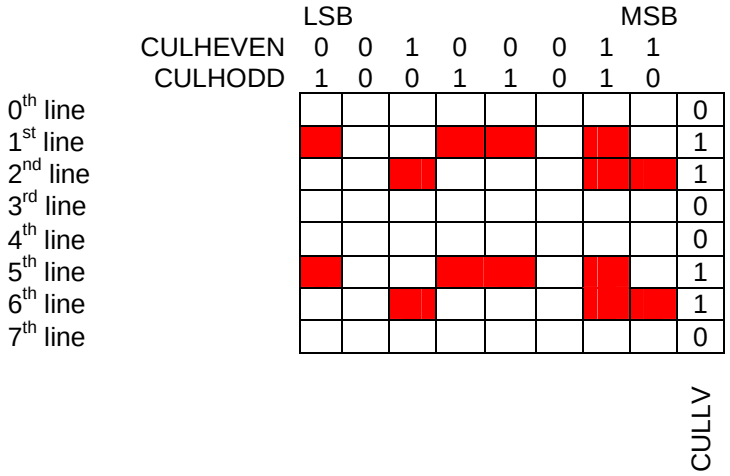


Figure 6: Example for Decimation Pattern

1.4.6.2 Output Format

The bits of data from each pixel are stored in the lower bits of a 16-bit SDRAM word, and the unused bit positions are filled with zeros. The SDRAM data format is shown in the Table 4.

	Lower word		Upper word	
	LSB(0)	MSB(15)	LSB(16)	MSB(31)
14bit	Pixel0	0	Pixel1	0
13bit	Pixel0	0	Pixel1	0
12bit	Pixel0	0	Pixel1	0
11bit	Pixel0	0	Pixel1	0
10bit	Pixel0	0	Pixel1	0
9bit	Pixel0	0	Pixel1	0
8bit	Pixel0	0	Pixel1	0
8bit pack	Pixel0	Pixel1	Pixel2	Pixel3

Table 4: SDRAM CCD Data Format

The processed CCD data is transferred to the SDRAM controller (SDRC) in units of 32 bytes. Data is transferred from the CCDC to the SDRC in 32-byte bursts.

Data is only written to SDRAM when WEN in SYNCEN is set to “1”.

The output formatter can be configured for any image format by using SDRAM line offset register - HSIZE, and offset register - SDOFST.

Figure 7 shows how to construct a frame format in SDRAM.

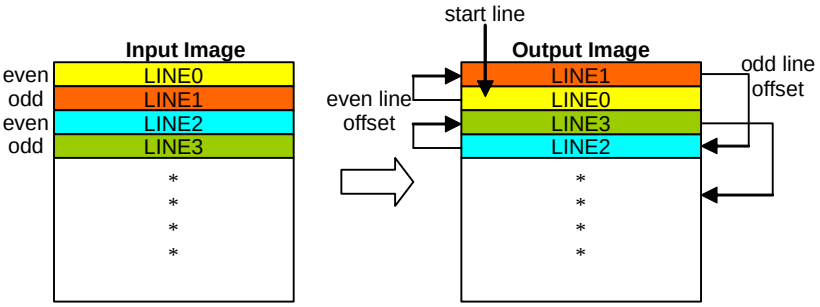


Figure 7: Frame Image format conversion

1.5 CCD Interrupts

The CCDC can generate two different interrupts VD0 and VD1.

1.5.1 Interrupts VD0 and VD1

As shown in the Figure 8, the VD0 and VD1 interrupts occur relative to the VD pulse. VD0 and VD1 will occur after receiving the number of horizontal lines (horizontal pulse signals) set in *VDINT0 and VDINT1* respectively.

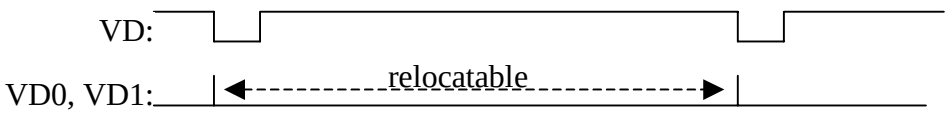


Figure 8: CCDC VD0, VD1 Interrupts

1.6 YCbCr signal Processing

Figure 9 shows YCbCr signal processing flow in the CCD controller block. The CCD controller accepts 4:2:2 sampled YCbCr input data. The luminance and color difference signals are each 8 bits, scaled 0 to 255. The color difference signals are multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input parallel(16-bit mode) or may be time multiplexed and input as a single bus(8-bit mode). The single bus may also contain SAV and EAV video timing reference codes(ITU-R BT.656 mode). In CCIR656 mode, the CCD controller is controlled by the SAV(Start Active Video) time code in the 8-bit pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. DM320 decodes SAV code and is synchronized at this timing.

The 16-bit or 8-bit YCbCr data is stored in SDRAM as 4:2:2 format. *Table 5* shows data format in SDRAM. Y data typically has a range of 16 to 235, however, it is possible to subtract a DC value to Y signal.

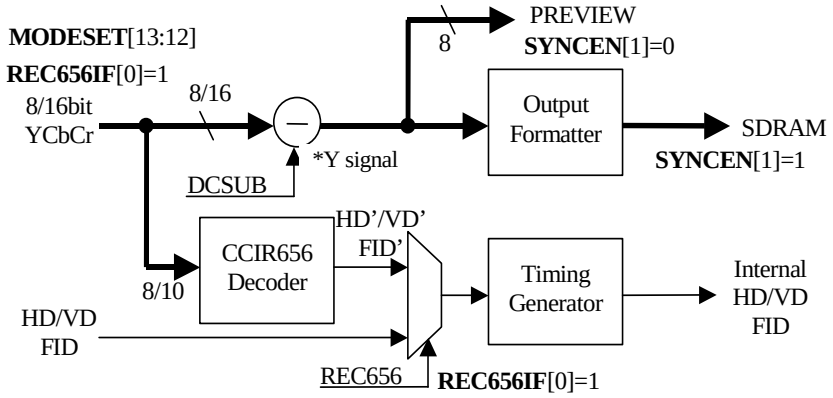


Figure 9: YCbCr signal processing

SDRAM Address	Lower word LSB(0)	Lower word MSB(15)	Upper word LSB(16)	Upper word MSB(31)
N	Cb0	Y0	Cr0	Y1
N+1	Cb2	Y2	Cr2	Y3
N+2	Cb4	Y4	Cr4	Y5

Table 5: SDRAM Data Format

1.7 Input/Output port configuration

DM320 supports several port configurations as shown in the Figure 10. Input / Output port configuration and byte swapping of input/output port or input data through is configurable by setting *CCDCFG* register.

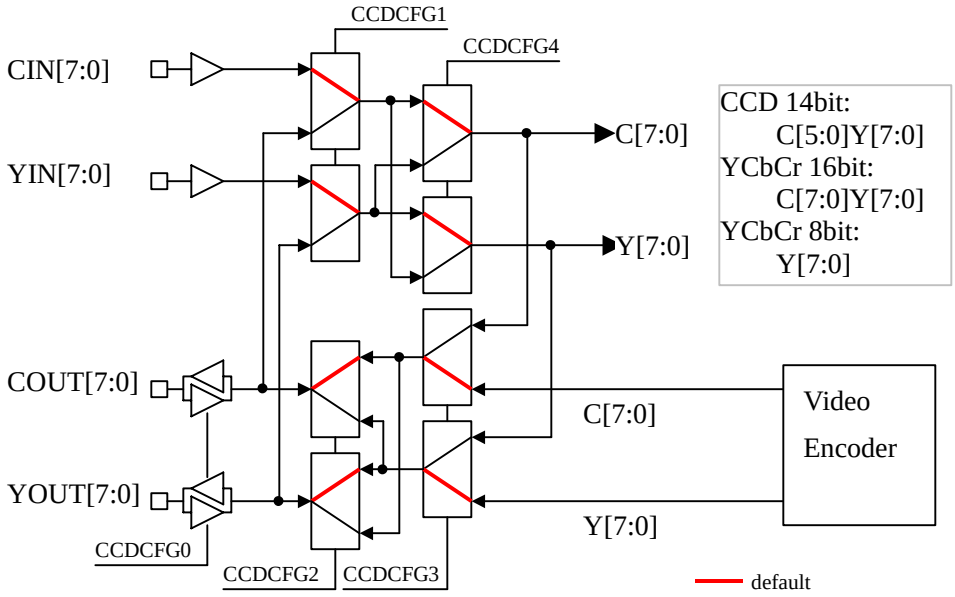


Figure 10: Video Port Configuration

1.8 CCIR-656 4:2:2 Parallel Interface

The CCIR-656 signal interface is shown in Figure 11. CCIR-656 is a specification that provides a method to transfer YCbCr-4:2:2 formatted, digital video data over an 8/10-bit wide interface. Data and timing codes are transferred over the same 8/10-bit interface.

To enable CCIR-656 mode, set R656E in REC656IF register. When in CCIR-656 mode, only the data lines and clock signal are connected between the external device and the CCDC. An NTSC/PAL decoder is an example of an external device that may be connected to the CCIR-656 interface.

Data lines Y7-Y0 are used for 8-bit YCbCr data and data lines C1-C0, Y7-Y0 are used for 10-bit YcbCr data. The video timing signals, HD, VD, and FIELD, are generated internally by the CCDC.

At the start and end of each video data block the device sends a unique timing reference code. The start code is called the Start of Active Video signal (SAV), and the end code is called the End of Active Video signal (EAV). The SAV and EAV codes proceed and follow valid data as shown in Figure 11. HD, VD, and FIELD are generated internally by the CCDC based on the SAV and EAV codes. The delay between the end of the HD pulse and the start of valid data can be

configured by setting SPH and the length of valid data can be configured by setting NPH .

Both timing reference signals, SAV and EAV, consist of a four word sequence in the following format: FF 00 00 XY, where FF 00 00 are a set preamble and the fourth word defines the field identification, the state of vertical field blanking, the state of horizontal line blanking, and error correction codes. The bit format of the fourth word is shown in *Table 6* and the definitions for bits, F, V, and H, are given in *Table 7* . F, V, and H are used in place of the usual horizontal sync, vertical sync, and blank timing control signals. Bits P3, P2, P1, and P0 are error correction bits for F, V, and H. The relationship between F, V, and H and the error correction bits is given in *Table 8*.To enable error correction, set bit ECCFVH in *REC656IF* . The CCDC will automatically detect and apply error correction when ECCFVH is enabled.

Note: the CCIR-656 specification is for 525-line and 625-line, digital component video signals in compliance with CCIR Rec. 601. Please refer to CCIR document Rec. 656-1 for detailed information on the interface.

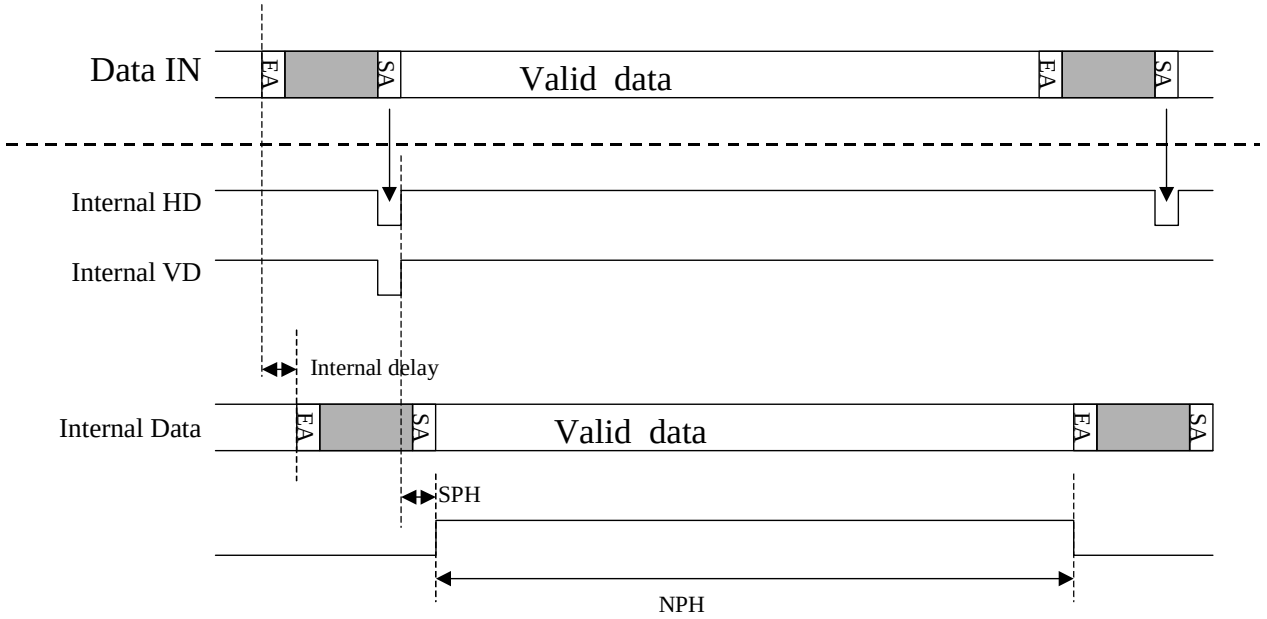


Figure 11: CCIR-656 Signal Interface

Data Bit Number	First Word	Second Word	Third Word	Fourth Word
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P1
4	1	0	0	P2
3	1	0	0	P3
2	1	0	0	P4
1	1	0	0	0

Data Bit Number	First Word	Second Word	Third Word	Fourth Word
0	1	0	0	0

Table 6: Video Timing Reference Codes for SAV and EAV

Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

Table 7: F, V, H Signal Descriptions

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	1
0	1	1	1	1	1	0
1	0	0	0	1	1	1
1	0	1	0	0	1	0
1	1	0	1	1	0	0
1	1	1	1	0	0	1

Table 8: F, V, H Error Correction Bits

When operating in CCIR-656 mode, data is stored in SDRAM according to the format shown in the *Figure 12.*

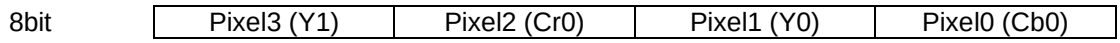


Figure 12: CCIR-656 mode data format in SDRAM

1.9 CCDC Register Update Timing

Many of the CCDC registers contain bits that are latched by the VD signal. Data written to a latched bit does not take affect until the next VD pulse is received. This allows registers that control the CCDC, such as the SDRAM write address location, HD width, VD width, etc. to be changed in between successive VD pulses without corrupting the current frame of CCD data. The CCDC registers, latched by the VD signal are, SYNCEN, LPF, bit 14 in MODESET, HDWIDTH, VDWIDTH, PPLN, LPFR, SPH, NPH, SLV0, SLV1, NLV, CULH, CULV,HSIZE, SDOFST, STADRH, STADRL, CLAMPEN bit in CLAMP and GAMMAWD.

Other CCDC registers are asynchronously set up with VD.

1.10 CCD Controller Register Map (CCDC)

Address	Register	Description
00031700	SYNCEN	Synchronization Enable
00031702	MODESET	Mode Setup
00031704	HDWIDTH	HD pulse width
00031706	VDWIDTH	VD pulse width
00031708	PPLN	Pixels per line
0003170A	LPFR	Lines per frame
0003170C	SPH	Start pixel horizontal
0003170E	NPH	Number of pixels horizontal
00031710	SLV0	Start line vertical - field 0
00031712	SLV1	Start line vertical - field 1
00031714	NLV	Number of lines vertical
00031716	CULH	Culling - horizontal
00031718	CULV	Culling - vertical
0003171A	HSIZE	Horizontal size
0003171C	SDOFST	SDRAM Line Offset
0003171E	STADRH	SDRAM Address #1 - high
00031720	STADRL	SDRAM Address #2 - low
00031722	CLAMP	CCD Data Clamping
00031724	DCSUB	DC Clamp
00031726	COLPTN	CCD Color Pattern
00031728	BLKCMP0	Black Compensation #1
0003172A	BLKCMP1	Black Compensation #2
0003172C	MEDFILT	CCD Median Filter
0003172E	RYEGAIN	CCD Gain Adjustment
00031730	GRCYGAIN	CCD Gain Adjustment
00031732	GBGGAIN	CCD Gain Adjustment
00031734	BMGGAIN	CCD Gain Adjustment
00031736	OFFSET	CCD Offset Adjustment
00031738	OUTCLIP	Output Clipping Value
0003173A	VDINT0	VD Interrupt #0
0003173C	VDINT1	VD Interrupt #1
0003173E	RSV0	Reserved
00031740	GAMMAWD	Gamma Correction settings
00031742	REC656IF	CCIR 656 Control
00031744	CCDCFG	CCD Configuration
00031746	FMTCFG	CCD Formatter configuration
00031748	FMTSPH	CCD Formatter - Start pixel horiz
0003174A	FMTLNH	CCD Formatter - number of pixels
0003174C	FMTSLV	CCD Formatter - start line vertical
0003174E	FMTLNV	CCD Formatter - number of lines
00031750	FMTOFST	CCD Formatter - Offset
00031752	FMTRLEN	CCD Formatter - Read out lines
00031754	FMTHCNT	CCD Formatter - HSYNC cycles
00031756	FMTPTNA	CCD Formatter - Culling patter A
00031758	FMTPTNB	CCD Formatter - Culling patter B

1.11 CCD Controller Registers

1.11.1 SYNCEN

CCDC Synchronization Enable

SYNCEN 0003:0700 offset: 0x00 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	WEN	VDHDEN
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:2	RSV			Reserved
1	WEN	0	R/W	Data Write Enable » 0: disable « » 1: enable « *Controls whether or not CCD raw data is written to SDRAM. *This bit is latched by VD.*
0	VDHDEN	0	R/W	VD/HD Enable » 0: disable « » 1: enable « *If VD/HD are defined as output, activates internal timing generator. If VD/HD are defined as inputs, activates internal timing generator to synchronize with VD/HD.*

1.11.2 MODESET

CCDC Mode Setup

MODESET 0003:0702 offset: 0x02 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FLDSTAT	LPF	IMPMOD[1]	IMPMOD[0]	PACK8	DATSIZ[2]	DATSIZ[1]	DATSIZ[0]	FLDMODE	DATAPOL	EXWEN	FLDPOL	HDPOL	VDPOL	FLDOUT	VDHDOUT
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	FLDSTAT	0	R	Field Status » 0: odd field « » 1: even field «
14	LPF	0	R/W	3-tap Low-Pass (anti-aliasing) Filter » 0: off « » 1: on «
13:12	IMPMOD	0	R/W	Setting of data input mode » 0: CCD RAW data « » 1: YCbCr 16-bit « » 2: YCbCr 8-bit « » 3: Reserved «
11	PACK8	0	R/W	Pack to 8-bits/pixel » 0: normal (16 bits/pixel) « » 1: pack to 8-bits/pixel «
10:8	DATSIZ	0	R/W	CCD Data Width » 000: 14-bits « » 001: 13-bits « » 010: 12-bits « » 011: 11-bits « » 100: 10-bits « » 101: 9-bits « » 110: 8-bits « » 111: Reserved «
7	FLDMODE	0	R/W	Sensor Field Mode » 0: non-interlaced (progressive) « » 1: interlaced «
6	DATAPOL	0	R/W	CCD Data Polarity » 0: normal (no change) « » 1: one's complement «
5	EXWEN	0	R/W	External WEN Selection » 0: do not use external WEN (Write Enable) « » 1: use external WEN (Write Enable) « To write CCD data to SDRAM
4	FLDPOL	0	R/W	Field Indicator Polarity » 0: postive « » 1: negative «
3	HDPOL	0	R/W	HD Sync Polarity » 0: postive « » 1: negative «
2	VDPOL	0	R/W	VD Sync Polarity » 0: postive « » 1: negative «
1	FLDOUT	0	R/W	Field ID Direction » 0: input « » 1: output «
0	VDHDOUT	0	R/W	VD/HD Sync Direction » 0: input « » 1: output «

1.11.3 HDWIDTH

CCDC HD pulse width

HDWIDTH 0003:0704 offset: 0x04 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HDW[11]	HDW[10]	HDW[9]	HDW[8]	HDW[7]	HDW[6]	HDW[5]	HDW[4]	HDW[3]	HDW[2]	HDW[1]	HDW[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HDW	0	R/W	Width of HD sync pulse if output: HDW+1 pixel clocks *HDWIDTH is not used when HD is input, i.e when VDHDOUT in MODESET is cleared to '0'.* **This bit field is latched by VD.*

1.11.4 VDWIDTH

CCDC VD pulse width

VDWIDTH 0003:0706 offset: 0x06 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VDW[11]	VDW[10]	VDW[9]	VDW[8]	VDW[7]	VDW[6]	VDW[5]	VDW[4]	VDW[3]	VDW[2]	VDW[1]	VDW[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VDW	0	R/W	Width of VD sync pulse if output: VDW+1 lines VDWIDTH is not used when VD is input, i.e when VDHDOUT in MODESET is cleared to '0'. **This bit field is latched by VD.*

1.11.5 PPLN

CCDC Pixels per line

PPLN 0003:0708 offset: 0x08 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PPLN[15]	PPLN[14]	PPLN[13]	PPLN[12]	PPLN[11]	PPLN[10]	PPLN[9]	PPLN[8]	PPLN[7]	PPLN[6]	PPLN[5]	PPLN[4]	PPLN[3]	PPLN[2]	PPLN[1]	PPLN[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	PPLN	0	R/W	Pixels per line - number of pixel clock periods in one line HD period = PPLN+1 pixel clocks PPLN is not used when HD and VD are inputs, i.e when VDHDOUT in MODESET is cleared to '0'. *This bit field is latched by VD.

1.11.6 LPFR

CCDC Lines per frame

LPFR 0003:070A offset: 0x0A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HLPFR[15]	HLPFR[14]	HLPFR[13]	HLPFR[12]	HLPFR[11]	HLPFR[10]	HLPFR[9]	HLPFR[8]	HLPFR[7]	HLPFR[6]	HLPFR[5]	HLPFR[4]	HLPFR[3]	HLPFR[2]	HLPFR[1]	HLPFR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	HLPFR	0	R/W	Half lines per filed or frame - sets number of half lines per frame or field. VD period = (HLPFR+1)/2 lines LPFR is not used when HD and are inputs, i.e when VDHDOUT in MODESET is cleared to '0'. *This bit field is latched by VD.

1.11.7 SPH

CCDC Start pixel horizontal

SPH 0003:070C offset: 0x0C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	SPH[14]	SPH[13]	SPH[12]	SPH[11]	SPH[10]	SPH[9]	SPH[8]	SPH[7]	SPH[6]	SPH[5]	SPH[4]	SPH[3]	SPH[2]	SPH[1]	SPH[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	SPH	0	R/W	Start pixel, horizontal Sets pixel clock position at which data output to SDRAM begins, measured from the start of HD **This bit field is latched by VD.*

1.11.8 NPH

CCDC Number of pixels horizontal

NPH 0003:070E offset: 0x0E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	NPH[14]	NPH[13]	NPH[12]	NPH[11]	NPH[10]	NPH[9]	NPH[8]	NPH[7]	NPH[6]	NPH[5]	NPH[4]	NPH[3]	NPH[2]	NPH[1]	NPH[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	NPH	0	R/W	Number of pixels, horizontal Sets number of horizontal pixels that will be output to SDRAM = (NPH + 1) '&' 0xFFF0, i.e. the number of horizontal output pixels is truncated to multiples of 16. **This bit field is latched by VD.*

1.11.9 SLV0

CCDC Start line vertical - field 0

SLV0 0003:0710 offset: 0x10 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	SLV0[14]	SLV0[13]	SLV0[12]	SLV0[11]	SLV0[10]	SLV0[9]	SLV0[8]	SLV0[7]	SLV0[6]	SLV0[5]	SLV0[4]	SLV0[3]	SLV0[2]	SLV0[1]	SLV0[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	SLV0	0	R/W	Start Line, Vertical (Field 0) Sets line at which data output to SDRAM will begin, measured from the start of VD **This bit field is latched by VD.*

1.11.10 SLV1

CCDC Start line vertical - field 1

SLV1 0003:0712 offset: 0x12 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	SLV1[14]	SLV1[13]	SLV1[12]	SLV1[11]	SLV1[10]	SLV1[9]	SLV1[8]	SLV1[7]	SLV1[6]	SLV1[5]	SLV1[4]	SLV1[3]	SLV1[2]	SLV1[1]	SLV1[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	SLV1	0	R/W	Start Line, Vertical (Field 1) Sets line at which data output to SDRAM will begin, measured from the start of VD **This bit field is latched by VD.*

1.11.11 NLV

CCDC Number of lines vertical

NLV 0003:0714 offset: 0x14 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	NLV[14]	NLV[13]	NLV[12]	NLV[11]	NLV[10]	NLV[9]	NLV[8]	NLV[7]	NLV[6]	NLV[5]	NLV[4]	NLV[3]	NLV[2]	NLV[1]	NLV[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	NLV	0	R/W	Number of lines, vertical Sets number of vertical lines that will be output to SDRAM. The number of lines output to SDRAM = (NLV + 1). **This bit field is latched by VD.*

1.11.12 CULH

CCDC Culling - horizontal

CULH 0003:0716 offset: 0x16 default: 0xFFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CULHEVN[7]	CULHEVN[6]	CULHEVN[5]	CULHEVN[4]	CULHEVN[3]	CULHEVN[2]	CULHEVN[1]	CULHEVN[0]	CULHODD[7]	CULHODD[6]	CULHODD[5]	CULHODD[4]	CULHODD[3]	CULHODD[2]	CULHODD[1]	CULHODD[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Name	Reset Value	R/W	Function
15:8	CULHEVN	255	R/W	Horizontal Culling Pattern for Even Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain *LSB is first pixel, MSB is 8th pixel, then pattern repeats.* **This bit field is latched by VD.*
7:0	CULHODD	255	R/W	Horizontal Culling Pattern for Odd Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain *LSB is first pixel, MSB is 8th pixel, then pattern repeats.* **This bit field is latched by VD.*

1.11.13 CULV

CCDC Culling - vertical

CULV 0003:0718 offset: 0x18 default: 0x00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	CULV[7]	CULV[6]	CULV[5]	CULV[4]	CULV[3]	CULV[2]	CULV[1]	CULV[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	CULV	255	R/W	Vertical Culling Pattern, 8-bit mask: 0: cull, 1:retain *LSB is first line, MSB is 8th line, then pattern repeats.* **This bit field is latched by VD.*

1.11.14 HSIZE

CCDC Horizontal size

HSIZE 0003:071A offset: 0x1A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	LNOFST[11]	LNOFST[10]	LNOFST[9]	LNOFST[8]	LNOFST[7]	LNOFST[6]	LNOFST[5]	LNOFST[4]	LNOFST[3]	LNOFST[2]	LNOFST[1]	LNOFST[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	LNOFST	0	R/W	Address offset for each line. Sets size of line in SDRAM, units: 32 bytes Either 16 or 32 pixels depending on setting of PACK8 **This bit field is latched by VD.*

1.11.15 SDOFST

CCDC SDRAM Line Offset

SDOFST 0003:071C offset: 0x1C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	FIINV	FOFST[1]	FOFST[0]	LOFTS0[2]	LOFTS0[1]	LOFTS0[0]	LOFTS1[2]	LOFTS1[1]	LOFTS1[0]	LOFTS2[2]	LOFTS2[1]	LOFTS2[0]	LOFTS3[2]	LOFTS3[1]	LOFTS3[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14	FIINV	0	R/W	Field identification signal inverse » 0: Non inverse « » 1: Inverse «
13:12	FOFST	0	R/W	Line offset value of odd field (FID = 1) » 00: +1 line « » 01: +2 line « » 10: +3 line « » 11: +4 line «
11:9	LOFTS0	0	R/W	Line offset values of even line and even field (FID = 0) » 000: +1 line « » 001: +2 lines « » 010: +3 lines « » 011: +4 lines « » 100: -1 line « » 101: -2 lines « » 110: -3 lines « » 111: -4 lines «
8:6	LOFTS1	0	R/W	Line offset values of odd line and even field (FID = 0) » 000: +1 line « » 001: +2 lines « » 010: +3 lines « » 011: +4 lines « » 100: -1 line « » 101: -2 lines « » 110: -3 lines « » 111: -4 lines «
5:3	LOFTS2	0	R/W	Line offset values of even line and odd field (FID = 1) » 000: +1 line « » 001: +2 lines « » 010: +3 lines « » 011: +4 lines « » 100: -1 line « » 101: -2 lines « » 110: -3 lines « » 111: -4 lines «
2:0	LOFTS3	0	R/W	Line offset values of odd line and odd field (FID = 1) » 000: +1 line « » 001: +2 lines « » 010: +3 lines « » 011: +4 lines « » 100: -1 line « » 101: -2 lines « » 110: -3 lines « » 111: -4 lines «

1.11.16 STADRH

CCDC SDRAM high address

STADRH 0003:071E offset: 0x1E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADRH[6]	ADRH[5]	ADRH[4]	ADRH[3]	ADRH[2]	ADRH[1]	ADRH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	ADRH	0	R/W	Upper 7 bits of the SDRAM starting address for CCDC output The address is specified offset from the SDRAM base address in units of 32 bytes. *This bit field is latched by VD.*

1.11.17 STADRL

CCDC SDRAM low address

STADRL 0003:0720 offset: 0x20 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADRL[15]	ADRL[14]	ADRL[13]	ADRL[12]	ADRL[11]	ADRL[10]	ADRL[9]	ADRL[8]	ADRL[7]	ADRL[6]	ADRL[5]	ADRL[4]	ADRL[3]	ADRL[2]	ADRL[1]	ADRL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	ADRL	0	R/W	Lower 16 bits of the SDRAM starting address for CCDC output The address is specified offset from the SDRAM base address in units of 32 bytes. *This bit field is latched by VD.*

1.11.18 CLAMP

CCD Data Clamping

CLAMP 0003:0722 offset: 0x22 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAMPEN	OBSLEN	OBSLN	OBST[12]	OBST[11]	OBST[10]	OBST[9]	OBST[8]	OBST[7]	OBST[6]	OBST[5]	OBST[4]	OBST[3]	OBST[2]	OBST[1]	OBST[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	CLAMPEN	0	R/W	Clamp Enable: » 0: disable « » 1: enable « Enables clamping of CCD data based on the calculated average of Optical Black Samples. *This bit is latched by VD.
14	OBSLEN	0	R/W	Optical Black Sample Length: » 0: 8 pixels « » 1: 16 pixels « Number of Optical Black Sample pixels per line to include in the average calculation.
13	OBSLN	0	R/W	Optical Black Sample Lines: » 0: 8 lines « » 1: 16 lines « Number of Optical Black Sample lines to include in the average calculation.
12:0	OBST	0	R/W	Start Pixel of Optical Black Samples Start pixel position of Optical Black Samples, specified from the start of HD in pixel clocks.

1.11.19 DCSUB

CCDC DC Clamp

DCSUB 0003:0724 offset: 0x24 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	DCSUB[13]	DCSUB[12]	DCSUB[11]	DCSUB[10]	DCSUB[9]	DCSUB[8]	DCSUB[7]	DCSUB[6]	DCSUB[5]	DCSUB[4]	DCSUB[3]	DCSUB[2]	DCSUB[1]	DCSUB[0]
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	RSV			Reserved
13:0	DCSUB	0	R/W	DC level to subtract from CCD data The DC value set here is subtracted from the CCD data when OBS clamping is disabled, CLAMPEN is 0

1.11.20 COLPTN

CCD Color Pattern

COLPTN 0003:0726 offset: 0x26 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPELPC0[1	CPELPC0[0	CPELPC1[1	CPELPC1[0	CPELPC2[1	CPELPC2[0	CPELPC3[1	CPELPC3[0	CPOLPC0[1	CPOLPC0[0	CPOLPC1[1	CPOLPC1[0	CPOLPC2[1	CPOLPC2[0	CPOLPC3[1	CPOLPC3[0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	CPELPC0	0	R/W	Color Pattern for Even Line, Pixel counter = 0 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
13:12	CPELPC1	0	R/W	Color Pattern for Even Line, Pixel counter = 1 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
11:10	CPELPC2	0	R/W	Color Pattern for Even Line, Pixel counter = 2 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
9:8	CPELPC3	0	R/W	Color Pattern for Even Line, Pixel counter = 3 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
7:6	CPOLPC0	0	R/W	Color Pattern for Odd Line, Pixel counter = 0 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
5:4	CPOLPC1	0	R/W	Color Pattern for Odd Line, Pixel counter = 1 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
3:2	CPOLPC2	0	R/W	Color Pattern for Odd Line, Pixel counter = 2 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «
1:0	CPOLPC3	0	R/W	Color Pattern for Odd Line, Pixel counter = 3 » 00: R/Ye « » 01: Gr/Cy « » 10: Gb/G « » 11: B/Mg «

1.11.21 BLKCMP0

Black Compensation #0

BLKCMP0 0003:0728 offset: 0x28 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_YE[7]	R_YE[6]	R_YE[5]	R_YE[4]	R_YE[3]	R_YE[2]	R_YE[1]	R_YE[0]	GR_CY[7]	GR_CY[6]	GR_CY[5]	GR_CY[4]	GR_CY[3]	GR_CY[2]	GR_CY[1]	GR_CY[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	R_YE	0	R/W	Black level compensation for R/Ye pixels (-128:+127) *2's complement, MSB is sign bit*
7:0	GR_CY	0	R/W	Black level compensation for Gr/Cy pixels (-128:+127) *2's complement, MSB is sign bit*

1.11.22 BLKCMP1

Black Compensation #1

BLKCMP1 0003:072A offset: 0x2A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GB_G[7]	GB_G[6]	GB_G[5]	GB_G[4]	GB_G[3]	GB_G[2]	GB_G[1]	GB_G[0]	B_MG[7]	B_MG[6]	B_MG[5]	B_MG[4]	B_MG[3]	B_MG[2]	B_MG[1]	B_MG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	GB_G	0	R/W	Black level compensation for Gb/G pixels (-128:+127) *2's complement, MSB is sign bit*
7:0	B_MG	0	R/W	Black level compensation for B/Mg pixels (-128:+127) *2's complement, MSB is sign bit*

1.11.23 MEDFILT

CCD Median Filter

MEDFILT 0003:072C offset: 0x2C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	MFTHR[13]	MFTHR[12]	MFTHR[11]	MFTHR[10]	MFTHR[9]	MFTHR[8]	MFTHR[7]	MFTHR[6]	MFTHR[5]	MFTHR[4]	MFTHR[3]	MFTHR[2]	MFTHR[1]	MFTHR[0]
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	RSV			Reserved
13:0	MFTHR	0	R/W	Threshold value for median filter

1.11.24 RYE GAIN

CCD RYE Gain Adjustment

RYEGAIN 0003:072E offset: 0x2E default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	GAIN	256	R/W	Gain adjustment factor for CCD data Value is U11Q8, i.e., decimal point between bits 8 and 7 Range: 0 - 7.9921875

1.11.25 GRCY GAIN

CCD GRCY Gain Adjustment

GRCYGAIN 0003:0730 offset: 0x30 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	GAIN	256	R/W	Gain adjustment factor for CCD data Value is U11Q8, i.e., decimal point between bits 8 and 7 Range: 0 - 7.9921875

1.11.26 GBG GAIN

CCD GBG Gain Adjustment

GBGGAIN 0003:0732 offset: 0x32 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	GAIN	256	R/W	Gain adjustment factor for CCD data Value is U11Q8, i.e., decimal point between bits 8 and 7 Range: 0 - 7.9921875 (2**3 - 2**-7) *Data is subsequently clipped to 13 bits*

1.11.27 BMG GAIN

CCD BMG Gain Adjustment

BMGGAIN 0003:0734 offset: 0x34 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	GAIN	256	R/W	Gain adjustment factor for CCD data Value is U11Q8, i.e., decimal point between bits 8 and 7 Range: 0 - 7.9921875

1.11.28 OFFSET

CCD Offset Adjustment

OFFSET 0003:0736 offset: 0x36 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]	OFFSET[2]	OFFSET[1]	OFFSET[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	OFFSET	0	R/W	Offset adjustment after gain adjustment Value is added to data after gain (0-1023)

1.11.29 OUTCLIP

CCDC Output Clipping Value

OUTCLIP 0003:0738 offset: 0x38 default: 0x3FFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	OCLIP[13]	OCLIP[12]	OCLIP[11]	OCLIP[10]	OCLIP[9]	OCLIP[8]	OCLIP[7]	OCLIP[6]	OCLIP[5]	OCLIP[4]	OCLIP[3]	OCLIP[2]	OCLIP[1]	OCLIP[0]
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Name	Reset Value	R/W	Function
15:14	RSV			Reserved
13:0	OCLIP	16383	R/W	Output clipping value for the final stage of CCD processing

1.11.30 VDINT0

CCDC VD Interrupt #0

VDINT0 0003:073A offset: 0x3A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	VDINT0[14]	VDINT0[13]	VDINT0[12]	VDINT0[11]	VDINT0[10]	VDINT0[9]	VDINT0[8]	VDINT0[7]	VDINT0[6]	VDINT0[5]	VDINT0[4]	VDINT0[3]	VDINT0[2]	VDINT0[1]	VDINT0[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	VDINT0	0	R/W	VD0 Interrupt Timing Specify VDINT0 in units of horiziontal lines from the start of VD pulse.

1.11.31 VDINT1

CCDC VD Interrupt #1

VDINT1 0003:073C offset: 0x3C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	VDINT1[14]	VDINT1[13]	VDINT1[12]	VDINT1[11]	VDINT1[10]	VDINT1[9]	VDINT1[8]	VDINT1[7]	VDINT1[6]	VDINT1[5]	VDINT1[4]	VDINT1[3]	VDINT1[2]	VDINT1[1]	VDINT1[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:0	VDINT1	0	R/W	VD1 Interrupt Timing Specify VDINT1 in units of horizontal lines from the start of VD pulse.

1.11.32 GAMMAWD

CCDC CCD Gamma

GAMMAWD 0003:0740 offset: 0x40 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MFIL1[1]	MFIL1[0]	MFIL2[1]	MFIL2[0]	RSV	RSV	CFAP	GWDI[2]	GWDI[1]	GWDI[0]	H3ATBL	CCDTBL
R/W	-	-	-	-	R/W	R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	-	-	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:10	MFIL1	0	R/W	Median Filter for Preview Engine » 0: No Median filter « » 1: Average filter « » 2: Median filter « » 3: Reserved «
9:8	MFIL2	0	R/W	Median Filter for 3A, CCD capture » 0: No Median filter « » 1: Average filter « » 2: Median filter « » 3: Reserved «
7:6	RSV			Reserved
5	CFAP	0	R/W	CFA Pattern » 0: Mozaic « » 1: Stripe «
4:2	GWDI	0	R/W	Gamma Width Input (A-LAW table) » 000: bits 13-4 « » 001: bits 12-3 « » 010: bits 11-2 « » 011: bits 10-1 « » 100: bits 9-0 « Others: Reserved
1	H3ATBL	0	R/W	Apply Gamma (A-LAW) to CCDC data sent to Hardware 3A » 0: disable « » 1: enable «
0	CCDTBL	0	R/W	Apply Gamma (A-LAW) to CCDC data saved to SDRAM » 0: disable « » 1: enable «

1.11.33 REC656IF

CCDC REC 656 standard interface

REC656IF 0003:0742 offset: 0x42 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ECCFVH	R656ON
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:2	RSV			Reserved
1	ECCFVH	0	R/W	FVH Error Correction Enable » 0: disable « » 1: enable «
0	R656ON	0	R/W	REC656 Interface Enable » 0: disable « » 1: enable «

1.11.34 CCDCFG

CCD Configuration

CCDCFG 0003:0744 offset: 0x44 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDLC	MSBINVO	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG	FIDMD[1]	FIDMD[0]	BW656	YCINSWP	RSV	YCOUTSWP	IDS	RSV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	-
Default	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	-

Bit	Name	Reset Value	R/W	Function
15	VDLC	0	R/W	Enable synchronizing function registers on VSYNC » 0: Synchronized on VSYNC « » 1: Not Synchronized on VSYNC «
14	MSBINVO	0	R/W	MSB of Chroma signal output inverted » 0: normal « » 1: MSB inverted «
13	MSBINVI	0	R/W	MSB of Chroma input signal stored to SDRAM inverted » 0: normal « » 1: MSB inverted «
12	BSWD	0	R/W	Byte Swap Data stored to SDRAM » 0: normal « » 1: Swap Bytes «
11	Y8POS	0	R/W	Location of Y signal when YCbCr 8bit data is input » 0: even pixel « » 1: odd pixel «
10	EXTRG	0	R/W	External Trigger » 0: Disable « » 1: Enable «
9	TRGSEL	0	R/W	Signal that initializes SDRAM address when EXTRG = 1 » 0: WEN bit (SYNCEN register) « » 1: FID input port «
8	WENLOG	0	R/W	Specifies CCD valid area » 0: Internal valid signal & WEN signal is ANDed logically « » 1: Internal valid signal & WEN signal is Ored logically «
7:6	FIDMD	0	R/W	Setting of FID detection function » 00: FID signal is latched at the VSYNC timing « » 01: FID signal is not latched « » 10: FID signal is latched at edge of VD « » 11: FID signal is latched based on phase of VD and HD«
5	BW656	0	R/W	The data width in CCIR656 input mode » 0: 8-bits « » 1: 10-bits «
4	YCINSWP	0	R/W	Y input (YIN[7:0]) and C input (CIN[7:0]) are swapped » 0: YIN[7:0] = Y signal / CIN[7:0] = C signal « » 1: YIN[7:0] = C signal / CIN[7:0] = Y signal «
3	RSV			Reserved
2	YCOUTSWP	0	R/W	Y output (YOUT[7:0]) and C output (COUT[7:0]) are swapped » 0: YOUT[7:0] = Y signal / COUT[7:0] = C signal « » 1: YOUT[7:0] = C signal / COUT[7:0] = Y signal «
1	IDS	0	R/W	Selection of Y / C signal » 0: YIN[7:0] & CIN[7:0] « » 1: YOUT[7:0] & COUT[7:0] «
0	RSV			Reserved

1.11.35 FMTCFG

CCDC FMT Configuration

FMTCFG 0003:0746 offset: 0x46 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	MOFST4[1]	MOFST4[0]	MOFST3[1]	MOFST3[0]	MOFST2[1]	MOFST2[0]	MOFST1[1]	MOFST1[0]	LNUM[1]	LNUM[0]	PNUM[1]	PNUM[0]	LNALT	FMTEN
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	RSV			Reserved
13:12	MOFST4	0	R/W	Offset value of write address at fourth line
11:10	MOFST3	0	R/W	Offset value of write address at third line
9:8	MOFST2	0	R/W	Offset value of write address at second line
7:6	MOFST1	0	R/W	Offset value of write address at first line
5:4	LNUM	0	R/W	Number of lines » 0: 1 line « » 1: 2 lines « » 2: 3 lines « » 3: 4 lines «
3:2	PNUM	0	R/W	Interval of i/p data format (Number of pixels) » 0: 1 pixel « » 1: 2 pixels « » 2: 3 pixels « » 3: 4 pixels «
1	LNALT	0	R/W	Line Alternating mode » 0: Normal mode « » 1: Line alternating mode «
0	FMTEN	0	R/W	CCD Formatter enable » 0: Off « » 1: On «

1.11.36 FMTSPH

CCDC FMT Start pixel horizontal

FMTSPH 0003:0748 offset: 0x48 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	FMTSPH[11]	FMTSPH[10]	FMTSPH[9]	FMTSPH[8]	FMTSPH[7]	FMTSPH[6]	FMTSPH[5]	FMTSPH[4]	FMTSPH[3]	FMTSPH[2]	FMTSPH[1]	FMTSPH[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTSPH	0	R/W	Start pixel horizontal

1.11.37 FMTLNH

CCDC FMT Numer of pixel horizontal

FMTLNH 0003:074A offset: 0x4A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	FMTLNH[11]	FMTLNH[10]	FMTLNH[9]	FMTLNH[8]	FMTLNH[7]	FMTLNH[6]	FMTLNH[5]	FMTLNH[4]	FMTLNH[3]	FMTLNH[2]	FMTLNH[1]	FMTLNH[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTLNH	0	R/W	Number of pixels in horizontal

1.11.38 FMTSLV

CCDC FMT Start line vertical

FMTSLV 0003:074C offset: 0x4C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	FMTSLV[11]	FMTSLV[10]	FMTSLV[9]	FMTSLV[8]	FMTSLV[7]	FMTSLV[6]	FMTSLV[5]	FMTSLV[4]	FMTSLV[3]	FMTSLV[2]	FMTSLV[1]	FMTSLV[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTSLV	0	R/W	Start line vertical

1.11.39 FMTLNV

CCDC FMT Number line vertical

FMTLNV 0003:074E offset: 0x4E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	FMTSLV[11]	FMTSLV[10]	FMTSLV[9]	FMTSLV[8]	FMTSLV[7]	FMTSLV[6]	FMTSLV[5]	FMTSLV[4]	FMTSLV[3]	FMTSLV[2]	FMTSLV[1]	FMTSLV[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTSLV	0	R/W	Number of lines in vertical

1.11.40 FMTOFST

CCDC FMT Offset adjustment

FMTOFST 0003:0750 offset: 0x50 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTOFST[1	MTOFST[1	FMTOFST[9	MTOFST[8	MTOFST[7	MTOFST[6	MTOFST[5	MTOFST[4	MTOFST[3	MTOFST[2	MTOFST[1	MTOFST[0
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTOFST	0	R/W	Offset for each line, memory size of each line

1.11.41 FMTRLEN

CCDC FMT Number of read-out lines

FMTRLEN 0003:0752 offset: 0x52 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTRLEN[1	MTRLEN[1	FMTRLEN[9	MTRLEN[8	MTRLEN[7	MTRLEN[6	MTRLEN[5	MTRLEN[4	MTRLEN[3	MTRLEN[2	MTRLEN[1	MTRLEN[0
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTRLEN	0	R/W	Number to be read out from line memory

1.11.42 FMTHCNT

CCDC FMT Horizontal sync interval

FMTHCNT 0003:0754 offset: 0x54 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTHCNT[1	MTHCNT[1	FMTHCNT[9	MTHCNT[8	MTHCNT[7	MTHCNT[6	MTHCNT[5	MTHCNT[4	MTHCNT[3	MTHCNT[2	MTHCNT[1	MTHCNT[0
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	FMTHCNT	0	R/W	HSYNC interval

1.11.43 FMTPTNA

CCDC FMT Culling pattern

FMTPTNA 0003:0756 offset: 0x56 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUL4EL[3]	CUL4EL[2]	CUL4EL[1]	CUL4EL[0]	CUL3EL[3]	CUL3EL[2]	CUL3EL[1]	CUL3EL[0]	CUL2EL[3]	CUL2EL[2]	CUL2EL[1]	CUL2EL[0]	CUL1EL[3]	CUL1EL[2]	CUL1EL[1]	CUL1EL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	CUL4EL	0	R/W	Culling pattern for line - 4 in even line
11:8	CUL3EL	0	R/W	Culling pattern for line - 3 in even line
7:4	CUL2EL	0	R/W	Culling pattern for line - 2 in even line
3:0	CUL1EL	0	R/W	Culling pattern for line - 1 in even line

1.11.44 FMTPTNB

CCDC FMT Culling pattern

FMTPTNB 0003:0758 offset: 0x58 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUL4OL[3]	CUL4OL[2]	CUL4OL[1]	CUL4OL[0]	CUL3OL[3]	CUL3OL[2]	CUL3OL[1]	CUL3OL[0]	CUL2OL[3]	CUL2OL[2]	CUL2OL[1]	CUL2OL[0]	CUL1OL[3]	CUL1OL[2]	CUL1OL[1]	CUL1OL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	CUL4OL	0	R/W	Culling pattern for line - 4 in odd line
11:8	CUL3OL	0	R/W	Culling pattern for line - 3 in odd line
7:4	CUL2OL	0	R/W	Culling pattern for line - 2 in odd line
3:0	CUL1OL	0	R/W	Culling pattern for line - 1 in odd line

2 Preview Engine

2.1 Introduction

The Preview Engine is a programmable hardware video processing module that generates image data in YCbCr-4:2:2 format from raw CCD data. The Preview Engine can also be configured to operate in a resize only mode, which allows the YCbCr-4:2:2 format data to be resized without applying the processing of every module in the Preview Engine.

The Preview Engine has the following features:

Supports Bayer, Sony VGA, and Foveon style patterns

Dual data input ports (CCD controller and SDRAM controller)

Noise filter with noise coring

Digital gain

White balance

Two steps smoothing

Horizontal and vertical seamless down sampling (x1/64~x1)

Horizontal and vertical seamless zoom (x1~x4),

Black adjustment

RGB2RGB blending matrix

Gamma correction

Luminance offset, brightness, and contrast

Chroma offset & suppression

Programmable RGB-to-YCbCr conversion coefficients

One-shot preview

Inverse A-Law table

Performs YCbCr-4:2:2 image resizing

Support 16bit data bus SDRAM

Histogram functionalities

Figure 13 shows the several modules that are used to process CCD raw data into YCbCr-4:2:2 data. These modules are described in detail in the later sections.

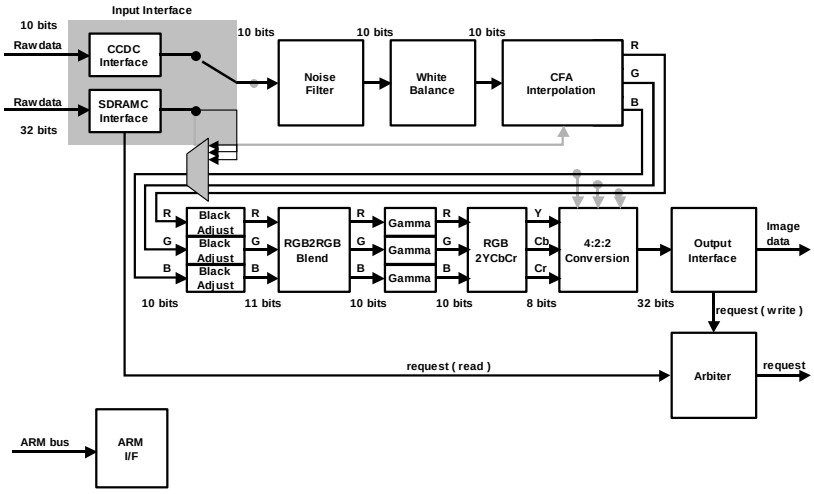


Figure 13: Block Diagram of the Preview Engine

2.2 Functional description

This section provides a detailed description of the modules that implement the Preview Engine's image pipeline. The module converts raw CCD data to YCbCr-4:2:2 data. The raw data input can come from the CCDC or from SDRAM. The YCbCr-4:2:2 output is always written to SDRAM.

See section 2.5 for description of fractional notation used in this chapter.

2.2.1 Color filter Array and Sensor Formats

A CCD sensor generates a color image by measuring the intensity of light that passes through a color filter mask. This color filter mask is called a Color Filter Array (CFA). The masking pattern of the CFA array as well as the filter color primaries vary between different manufactures. In digital camera applications, the filter color primaries are often components of the RGB or Complementary color space.

The Preview engine supports Sony and Foveon sensor formats in addition to the conventional Bayer pattern format. Figure 14 and

Figure 15 shows the Bayer and Foveon pattern respectvely. The configuration of the position of each RGB or complementary color component is done by PVSET2 register according to the CFA pattern used by the CCD module.

Note: DM320 does not support Sony VGA sensors in SDRAM input mode.

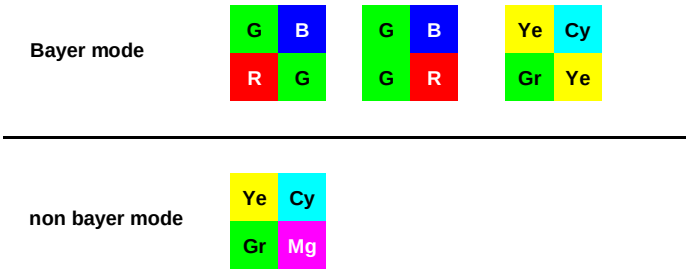


Figure 14: Conventional 2x2 CFA format

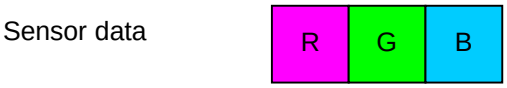


Figure 15: Foveon Sensor format

2.2.2 Noise Filter Module

The noise filter is the first image-processing step in the preview engine. It is useful to reduce an impulse noise present in the raw data from the CCD image sensor using a noise coring technique. When the NFEN bit in the NFILT register is 1, this noise filter is enabled and NFRT[1:0] bits in the NFILT register controls the gain of the high pass filter

2.2.3 White Balance Module

The preview engine white balance module has two gain adjusters, a digital gain adjuster and a white balance adjuster. In the digital gain adjuster, the raw data is multiplied by a fixed value gain regardless of the color pixel to be processed. This would affect the brightness of the image. The digital gain is configured in the DGAIN register. The format of DGAIN value is U10Q8.

In the white balance gain adjuster, the raw data is multiplied by a selected gain corresponding to the color of the processed pixel. While-balance parameters are configured in WBGAIN0 and WBGAIN1 registers. The format of WBGAINx registers is U8Q6.

Figure 16 shows the block diagram of the white balance module. It is composed of two multipliers for the digital gain and the white balance gain.

Note: The selection of the white balance gain depends on the type of sensor (conventional/converted Bayer or Foveon) and the color of the current pixel to be operated on.

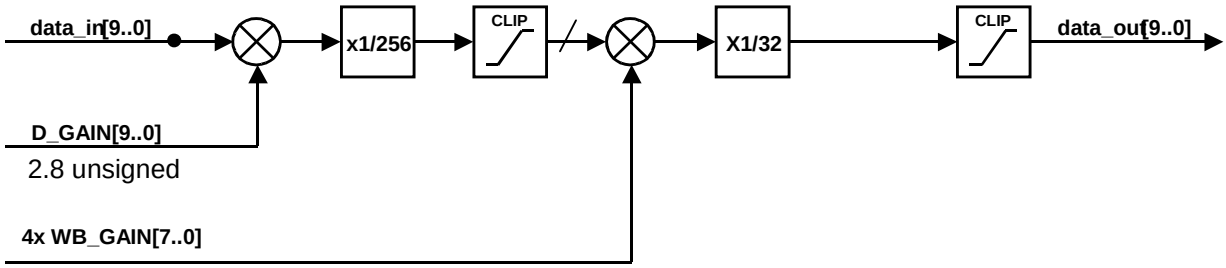


Figure 16: White Balance Module Block Diagram

2.2.4 CFA Interpolation

The Preview Engine's CFA interpolation modules perform functions such as, horizontal and vertical interpolation, smoothing, horizontal and vertical resizing, color adjustment and conversion from complementary to RGB color space. *Figure 17* shows a block diagram of the CFA interpolation module in normal mode. The dark lines shows the data path taken during normal mode.

When the Preview Engine is operating in resize only mode, some of the CFA interpolation modules are bypassed. In resize only mode, only smoothing and horizontal and vertical resizing are applied to the data. The data path taken in resize only mode is shown in shown by the dark lines in *Figure* 18.

The horizontal interpolation sub-module applies horizontal interpolation using a two tap or a five-tap interpolation filter.

A smoother sub-module performs a selectable low pass filter, which has 2 different levels of a bandwidth.

The horizontal re-sampler sub-module applies a seamless horizontal down-sampling or up-sampling (zoom) by x4 over-sampling.

The vertical interpolation and re-sampler sub-module performs a vertical interpolation and a seamless vertical down-sampling or up-sampling by x4 over-sampling using two line memories.

The color selector sub-module extracts the appropriate color from the 4 inputs of the vertical interpolation and re-sampler sub-module.

The color adjustment sub-module executes color adjustment on the interpolated data. This module is bypassed when the Preview Engine is in RGB CCD mode.

The comp2RGB conversion sub-module converts the data from the complementary color space to the RGB color space.

The output of the CFA interpolation module is RGB data regardless of a type of the color space used by the CCD imager.

In the case of the Foveon sensor, CFA interpolation is not necessary. Only the horizontal and vertical zoom circuitry in the CFA interpolation module should be active for the Foveon sensor. It is assumed that the Foveon sensor gives serial RGB data. Therefore, the RGB data needs to be buffered at the output of the CFA interpolation for feeding to the black adjustment module. In other words, all the stages following the CFA interpolation for the Foveon sensor will only

operate on one unique RGB data every three pixel clock cycles. To minimize power consumption, the buffer should transmit the same RGB pixel values for 3 consecutive pixel clock cycles. At the final output stage, the 2/3rd repetitive data need to be thrown away before writing to the SDRAM.

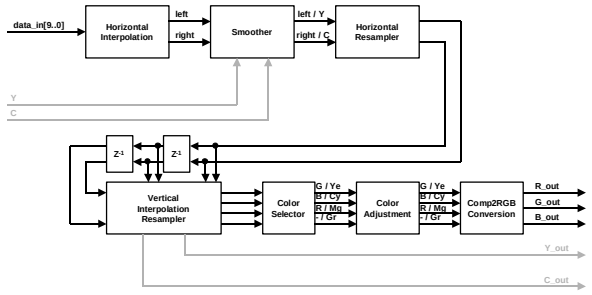


Figure 17: CFA Interpolation module (Normal Mode)

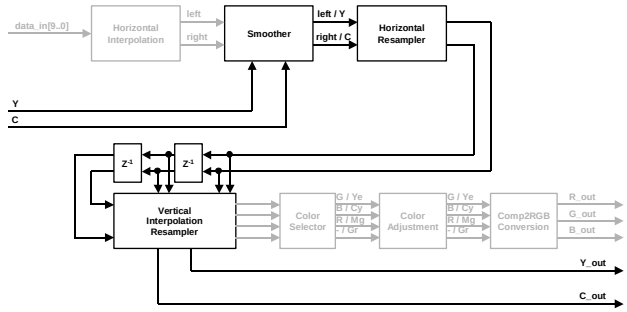


Figure 18 CFA Interpolation module (Resize only Mode)

2.2.4.1 Horizontal Interpolation

A horizontal interpolation sub-module performs a horizontal interpolation with a 2-tap or a 5-tap interpolation filter. The 2 taps interpolation filter uses an average of the next pixels on the left and right side of the pixel to be interpolated. On the other hand, the 5-tap interpolation filter utilizes the information of another color on the processed line so that a false color due to this interpolation process can be reduced effectively. Configure HINT bit in PVSET2 register for 2-tap or 5-tap interpolation.

2.2.4.2 Smoother

A smoother sub-module is an anti-aliasing filter that is composed of two kinds of FIR filters. By combining the two filters, one of two levels of horizontal low pass filter can be performed. The smoother sub-module (in Bayer mode) is composed of the two FIR filters and an output selector. The SMEN bit, SMLVL bit in the SMTH register determine the output.

2.2.4.3 Horizontal Re-sampler

A horizontal re-sampler sub-module performs a seamless horizontal down-sampling or up-sampling (zoom). This seamless re-sampling processing is done by a bi-linear interpolation of data from the smoother sub-module. *Figure 19* shows an example of this re-sampling process (x2 zoom in Bayer mode).

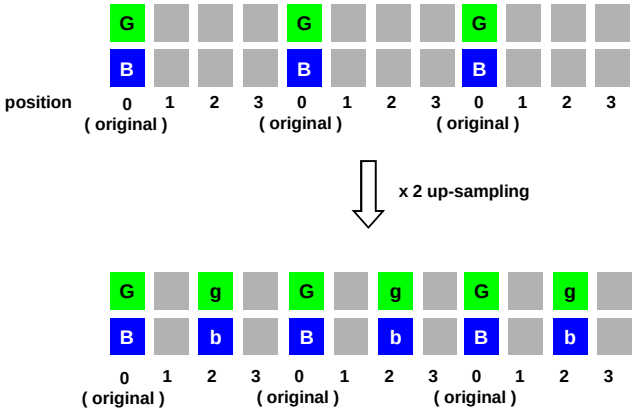


Figure 19: Example of the resampling (x2 up-sampling)

See section 2.4.3 for details about setting resizing registers.

2.2.4.4 Vertical Interpolation and Re-sampler

The vertical interpolation and re-sampler sub-module performs vertical interpolation and seamless vertical down-sampling or up-sampling.

Similar to horizontal resampler module, vertical resampling is done by a bi-linear interpolation of a data from the horizontal resampler sub-module and two line memories. And this sub-module executes two different calculations depending on the color pattern of CCD image sensor. *Figure 14* shows an example of two types of the CFA formats.

If the CFA pattern is of the type that has one color component in both lines, then this sub-module operates in bayer mode. Otherwise, this sub-module operates in non-bayer mode. In bayer mode, the vertical interpolation and resampling processing is based on the main color (G or Ye). As shown in *Figure 20*, in bayer mode one main color (G or Ye in this figure) exists in every line, and the other colors are calculated based on the main color.

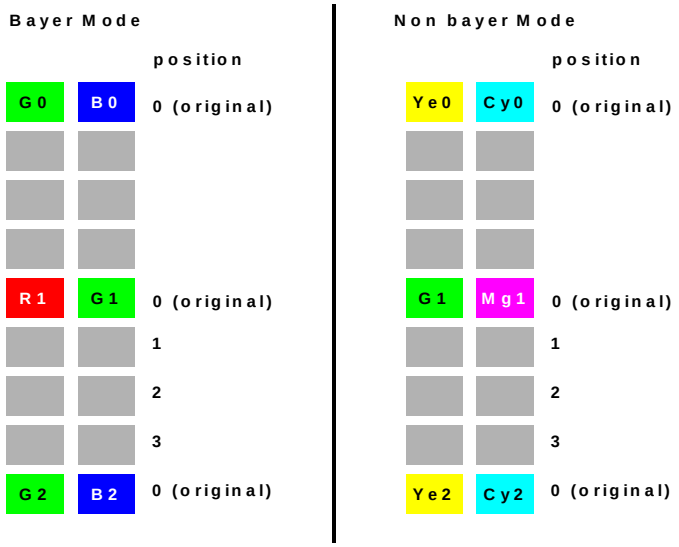


Figure 20: Comparison of inputs in Bayer mode and in non-Bayer mode

Note: Up-sampling is only possible when operating in SDRAM mode, i.e. when bit INMODE of PVSET1 register is set to 1.

2.2.4.5 Color Selector

The color selector sub-module extracts an appropriate color from the four input signals that the vertical interpolation and re-sampler sub-module generates. *Figure 21* shows a block diagram of the color selector sub-module. This extractor for each color selects an appropriate signal automatically using the sync signal and CFA [7:0] bits in the PVSET2 register.

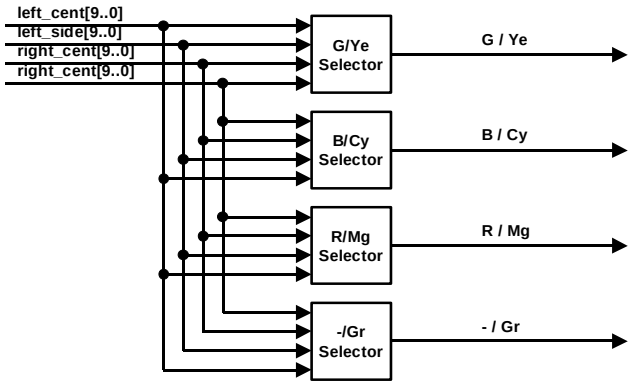


Figure 21: Block diagram of the color selector sub-module

2.2.4.6 Color Adjustment for the Complementary Color Space

The color adjustment sub-module performs the adjustment to interpolated data of 4 colors in the complementary color space in order to satisfy an equation of

the following complementary color space. If a CCDMOD bit in the PVSET2 register is zero, the data bypasses this sub-module.

2.2.4.7 Comp2RGB conversion

The comp2RGB conversion sub-module converts the data from four colors in the complementary color space to the RGB color space. Especially for G, data from the interpolation process and data calculated in this module using the same formula in the complementary color space can be blended. If the CCDMOD bit is 0, the data bypass this module.

2.2.5 Black Adjustment

After CFA interpolation, black adjustment can be applied to each color component, R, G, and B. A different offset can be applied to each component. The color adjustment sub-module performs the following calculation on each color component, as shown in *Figure 22*.

data_out = data_in + bl_offset

Black adjustment offset is specified as 8-bit 2's complement value and is set using BLOFST0 and BLOFST1 registers.

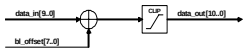


Figure 22: Block diagram of black adjuster module

2.2.6 RGB2RGB Blending Matrix

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3x3 square matrix transformation in combination with an added offset.

The registers MTXGAIN0 **-** MTXGAIN8 and MTXOFST0 - MTXOFST2 are used for RGB2RGB blending. Each of the gains is 12-bit data with a range of -8 to +8 (with 8-bit fraction).

The precision of MTXGAINx register is S12Q8. Offset is specified as 10-bit 2's complement number.

2.2.7 Gamma Correction and Y-enhancing table

The gamma correction can be done in two ways. One is to use an embedded ROM table. The second is to perform a gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. Each table has 128-entries, and each entry accommodates a 10-bit gain and 10-bit offset. The gamma correction module applies gamma correction to each color component, R, G and B. Set the bypass bits (BYPR, BYPG or BYPB) in GAMTSBYP register to bypass the gamma tables. The gamma tables can be bypassed for each color component, independently. In addition to Gamma tables for R, G and B, a table for non-linear enhancement of luminance component also can be setup.

From a software perspective each table has 256 entries of gain and offset. Gain and offset (10-bits each) needs to be setup separately. The address pointer increments by one for each write. All the four tables are linearly addressed. Thus there are 256 addresses in each table. The table address is set in

TABLE_ADDR register and the data is written in TABLE_DATA register. Table 9 illustrates the addressing of Gamma and Y-enhancing table.

Figure 23 shows a block diagram of the gamma correction module. When the BYPASS bit is asserted, the input data is passed as it is (10-bit precision). When the ROM is selected, the output of the ROM is eight bits, and two zeros are added at the LSB side to make it 10-bit.

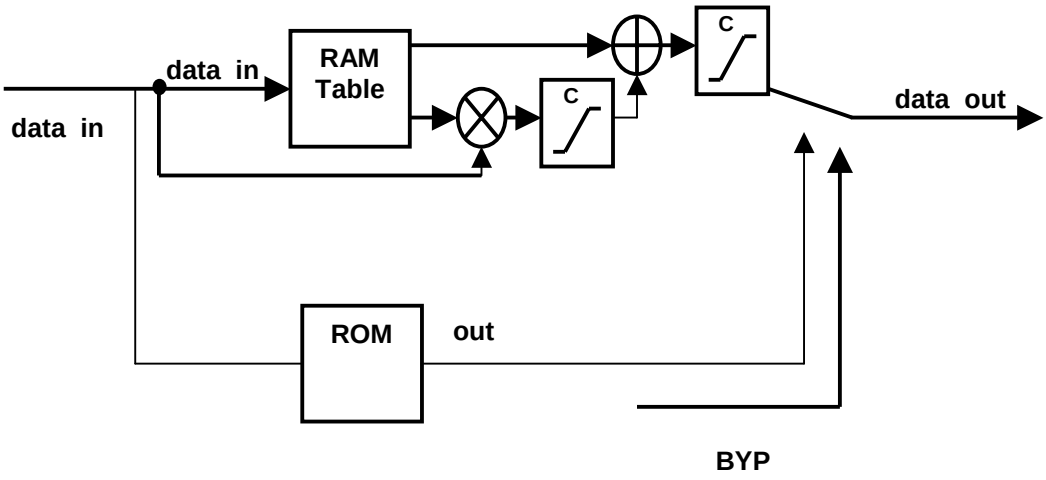


Figure 23: Gamma Correction Module Block Diagram

Gamma Table for Red	Address-0 (Gain)	Address-1 (Offset)
	…	…
	Address-254 (Gain)	Address-255 (Offset)
Gamma Table for Green	Address-256 (Gain)	Address-257 (Offset)
	…	…
	Address-510 (Gain)	Address-511 (Offset)
Gamma Table for Blue	Address-512 (Gain)	Address-513 (Offset)
	…	…
	Address-767 (Gain)	Address-768 (Offset)
Non-linear Y-enhancing table	Address-769 (Gain)	Address-770 (Offset)
	…	…
	Address-1022 (Gain)	Address-1023 (Offset)

Table 9: Gamma and Y-enhancing tables

2.2.8 RGB2YCbCr Conversion Module

The RGB2YCbCr conversion module has a 3x3 square matrix and converts the RGB color space of the image data into the YCbCr color space. In addition to the conversion matrix operation, offset, contrast, brightness and chroma suppression are performed in this module.

Register	Description
CSC0 -CSC4	Color Space Conversion Coefficient registers for RGB to Y, Cb, Cr conversion
YOFST	DC offset value for Y
COFST	DC offset value for Cb and Cr
CNTBRT	Contrast and brightness adjustment register for the Y data

Table 10: RGB to YCbCr conversion registers

The precision of CSCx register is S8Q6

In addition to this color space operation, contrast (scaling/multiplication) and brightness (offset/addition) adjustments can be made on the luminance data and pseudo-color suppression can be performed for chrominance data.

2.2.8.1 Pseudo-color suppression

The gain factor applied to Cb and Cr during pseudo-color suppression is determined using a configurable function mapping. The pseudo-color suppression can be enabled using CSUP0 register. The pseudo-color suppression threshold and gain can be set in the CSUP1 register. Use CSUPTH field to set the threshold constant and use CSUPG field to set the gain constant. Precision of CSUPG is U8Q8

Cgain is suppressed smaller than one while luminance signal level is higher than CSUPTH.

2.2.9 Output Clipping Module

Before outputting data to the SDRAM, Preview Engine performs clipping on the data. The minimum and maximum threshold values are specified using *SETUPY* and SETUPC registers**.** By default, these values are zero, so user needs to set appropriate value in order to get output from the preview engine. For example

0xFF for maximum Y, Cb, Cr value and 0 for minimum Y, Cb, Cr value means no clipping of output data

This setting must be done for all modes of operation including normal CCD raw-data processing mode, one-shot mode, resize only mode, SDRAM input mode.

2.2.10 4:2:2 Conversion and Output Interface Module

The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by discarding every other Cb and Cr component in the horizontal direction. After converting the data to YCbCr-4:2:2, the image data is transferred to the SDRAM controller (SDRC) in units of 32 bytes. The SDRC manages the transfer of the image data to SDRAM. The Preview Engine has an internal 16-bit by 16 FIFO that is used to buffer the data. Data is transferred from the FIFO to the SDRC in 32-byte bursts. *Figure 24* shows how the YCbCr image data is formatted in SDRAM

MSB		LSB	
31 24	23 16	15 8	7 0
Y1	Cr0	Y0	Cb0

Figure 24: YCbCr-4:2:2 Format

2.3 Histogram

Histogram function supports the following

- Up to 4 regions (areas)
  - Each region has separate on/off control
  - Each region has its own start coordinate X/Y (12-bit) and horizontal/vertical sizes (12-bit)
  - When the regions overlap, only one region is operated on (selected bin incremented)
- CFA data assumed (RGr lines and GbB lines interleaved). Foveon sensor is not supported, and data for each color go into separate set of bins
- Bins are counters, counting number of values in the range associated with the bins
- Per color, per region, there can be 32, 64, 128, or 256 bins
- Data values are first down-shifted then saturated for bin selection

2.3.1 Reset of Histogram RAM

The user is responsible for resetting the histogram RAM. This can be done by two ways.

- Writing zeros to the RAM via software
- If the CLR bit is set reading the memory will cause it to be reset after the read.

ARM reads and writes shall be blocked when the Start/Busy bit is 1

2.3.2 Illegal Setting Override

The histogram RAM is limited in size. Therefore the user can only set the number of bins as shown in Table 11

Regions	Bins allowed
1	256,128,64,32
1,2	128,64,32
1,2,3	64,32
1,2,3,4	64,32

Table 11: Regions and Bins for Histogram

2.3.3 Overflow Handling

If incrementing a histogram bin would cause the value to become greater than what the RAM word could hold, the value is saturated to the maximum value.

For eg, if the input data width is 10 bits (9 … 0) and the data to be histogrammed is 8 bits wide. Therefore, if the input value is larger than the highest bin location, the result shall be clipped to the highest bin location. This allows data from above the bin range to be included in the upper most bin.

Example:

1 Region enabled, 256 bins per color

Shift = 0, Pixel value = 1000

Pixel value (1000) > Max bin index (255)

Therefore the down-shifted pixel value is clipped to max bin index, 255, and bin 255 is incremented. If bin 255 already holds the maximum value, this incrementing is saturated so that the maximum value remains in the bin.

2.3.4 Region priority

Up to 4 regions can be active at any time but a pixel is only binned into one of regions. The priority is Region 0 > Region 1 > Region 2 > Region 3.

2.4 Preview Engine Operation Guide

This section explains how to configure and use the Preview Engine.

Some Preview Engine register bits are latched by the VD signal. The VD signal is the vertical synch pulse generated by the CCDC or input to the CCDC from an

external CCD imager. Data written to these latched registers does not take effect until the VD pulse is received. This allows bits that control the Preview Engine, such as the Preview Engine enable bit and the SDRAM data source and destination bit field, to be changed in between successive VD pulses without corrupting the current image being processed by the Preview Engine.

Incase of VD input mode (VDPOL and VDINT0 bits are set in CCDC module), preview engine registers are always latched on rising edge of the VD signal, irrespective of VD polarity, as shown in *Figure 25*.

When VD is output by CCDC, CCDC internally always generate VD signal with high polarity and before outputting the signal it inverts the VD based on VDPOL bit. Thus, when VD is output by CCDC, preview engine registers will always be latched at the start of VD.

Registers *PVEN, RSONLY bit in PVSET1* register*, RADRH, RADRL, WADRH, WADRL, HSTART, HSIZE,* VSTART*, and* VSIZE are latched by VD signal.

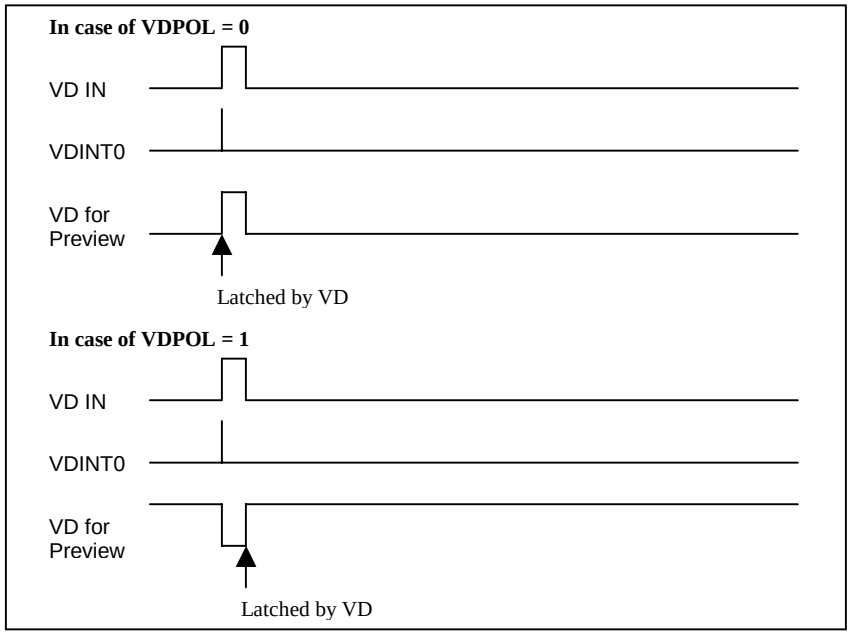


Figure 25: VD Polarity and Timing

2.4.1 Starting the Preview Engine

Setting PVEN bit of register PVEN activates the Preview Engine. Clearing this bit deactivates the Preview Engine. The status of the preview engine can be verified by reading PVEN bit. Also Preview Engine interrupt is generated when the preview engine changes from enabled state to disabled state. PVEN is latched by VD. PVEN timing is shown in *Figure* 26*.*

When PVEN bit is set, the Preview Engine becomes active at the next VD. When PVEN bit is cleared the Preview Engine becomes inactive after completing the last burst transfer of processed image data.

Furthermore when the Preview Engine becomes inactive the Preview Engine interrupt signal is issued. This interrupts always triggers after completing the last burst transfer of processed image data. Refer to chapter on “Interrupt Controller “for more information about this interrupt.

IMPORTANT: It is recommended that the preview engine is made inactive by clearing PVEN register when the following registers are being changed. PVSET1, HSRT, HSIZE, VSRT, VSIZE, SMTH, HRSZ, VRSZ

Preview Engine does not trigger Preview Engine interrupt after processing of each and every frame of data. It is triggered when

1. Preview Engine is disabled and last burst transfer of the last frame of processed image data is done
2. In one-shot mode, last burst transfer of the processed image data is done

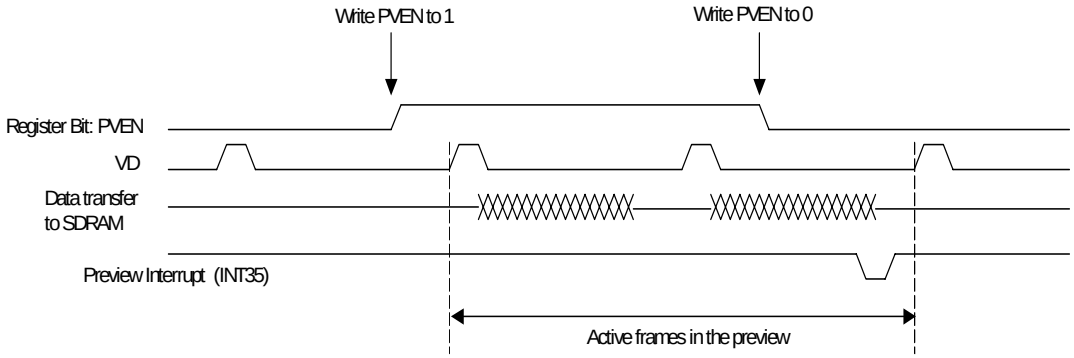


Figure 26: Preview Enable/disable timing

2.4.2 Preview Engine Input Modes

The preview engine has two selectable input ports, which are connected to the CCDC and the SDRAMC. There are some differences of available functions between the CCDC input mode and the SDRAMC input mode. Table 12, shows the main differences of available functions between the two input modes. Normal mode means RAW data input mode and Resize Only mode means YCbCr data input mode.

Functions for Bayer Sensor	CCDC input mode		SDRAMC input mode	
	Normal	Resize Only	Normal	Resize Only
Noise filter	Y	N	Y	N
Digital gain	Y	N	Y	N
White balance	Y	N	Y	N
Smoothing	Y	Y	Y	Y
Down sample	Y	Y	Y	Y
Zoom	N	N	Y	Y
RGB blend	Y	N	Y	N
Gamma	Y	N	Y	N
Chroma suppress	Y	N	Y	N
Chroma offset	Y	N	Y	N
1 shot preview	Y	Y	Y	Y
Histogram - Bayer	Y	N	Y	N
Black adjust	Y	N	Y	N

Table 12: Preview Engine: Input Mode Comparison for Bayer sensor

Functions for Foveon Sensor	CCDC input mode		SDRAMC input mode	
	Normal	Resize Only	Normal	Resize Only
Noise filter	Y	N	Y	N
Digital gain	Y	N	Y	N
White balance	Y	N	Y	N
Smoothing	Y	Y	Y	Y
Down sample	Y	Y	Y	Y
Zoom	N	N	Y	Y
RGB blend	Y	N	Y	N
Gamma	Y	N	Y	N
Chroma suppress	Y	N	Y	N
Chroma offset	Y	N	Y	N
1 shot preview	Y	Y	Y	Y
Histogram - Bayer	Y	N	Y	N
Black adjust	Y	N	Y	N

Table 13: Preview Engine: Input Mode Comparison for Foveon sensor

Functions for Sony VGA Sensor	CCDC input mode*	
	Normal	Resize Only
Noise filter	Y	N
Digital gain	Y	N
White balance	Y	N
Smoothing	Y	Y
Down sample	Y	Y
Zoom	N	N
RGB blend	Y	N
Gamma	Y	N
Chroma suppress	Y	N
Chroma offset	Y	N
1 shot preview	Y	Y
Histogram - Bayer	Y	N
Black adjust	Y	N

Table 14: Preview Engine: Input Mode Comparison for Sony VGA sensor

Note: Sony VGA sensor is not supported in SDRAM input mode

IMPORTANT: When Preview Engine is configured to take input from SDRAM (YCbCr input data during YCbCr resize or raw data input), in order for Preview Engine to operate the following conditions must be satisfied.

Set the VD mode to internal VD mode

SDRAM destination address must be specified. This is the location in SDRAM where the Preview Engine will write the processed image data.

When operating in SDRAM input mode, the user must also specify an SDRAM input data address. This is the location in SDRAM where the Preview Engine will read the data to be processed.

The SDRAM read/write address is specified as offset from start of SDRAM and in units of 32 bytes, since data is transferred between the Preview Engine and SDRAMC in bursts of 32 bytes.

For example suppose the SDRAM address 0x911000 is to be set as the Preview Engine write address, and 0x900000 is the SDRAM base Address, then the value that is to be programmed in the Preview Engine destination address registers (WADRL, WADRH) is calculated as follows:

(0x911000 – 0x900000)/32 = (0x11000)/32 = 0x880

When Preview Engine is configured to take input from SDRAM, the register HSTART must be set with the pixel width of input data present in the SDRAM

Furthermore, if the BSTAL bit is set to 1 in PVSET1 register, then the horizontal size of pixel data transferred to the SDRAMC will be aligned on a 32-byte boundary, i.e. if the horizontal size is not a multiple of 32-bytes, the excess data will not be transferred to the SDRAMC.

MAXY, MINY fields in register SETUPY and SETUPC, must be set. These registers specify the clipping to be applied to the Y, Cb, Cr pixel data before it is output to SDRAM.

2.4.2.1 SDRAM Input mode - input pixel width selection

The preview engine has three selectable modes in SDRAM input mode.

10bits mode (8BITS = 0 and ALAW =0 and INMODE = 1 in PVSET1 register)

8bits mode (8BITS = 1 and ALAW =0 and INMODE = 1 in PVSET1 register)

Inverse A-law mode (8BITS = 1 and ALAW =1 and INMODE = 1 in PVSET1 register).

NOTE: Inverse A-law mode is available only when preview engine is in SDRAM input mode. 10bits mode and 8bits mode is available in both SDRAM input mode as well as CCDC input mode

10bits mode

In 10bits mode, raw data must be stored in SDRAM as shown below,

31 24	23 16	15 8	7 0
x x x x	Pixel N+1 (25:16)	x x x x	Pixel N (9:0)

X = invalid bits

8bits mode

In this mode each input raw data pixel has width of 8bits. The raw data stored in SDRAM as shown below

31 24	23 16	15 8	7 0
Pixel N+3	Pixel N+2	Pixel N+1	Pixel N

Internally preview engine always processes raw data with 10 bits per pixel. When processing the 8-bit raw data, the preview engine expands the data from 8 bits to 10 bits by adding “00” in LSB side as shown in the *Figure 27*.

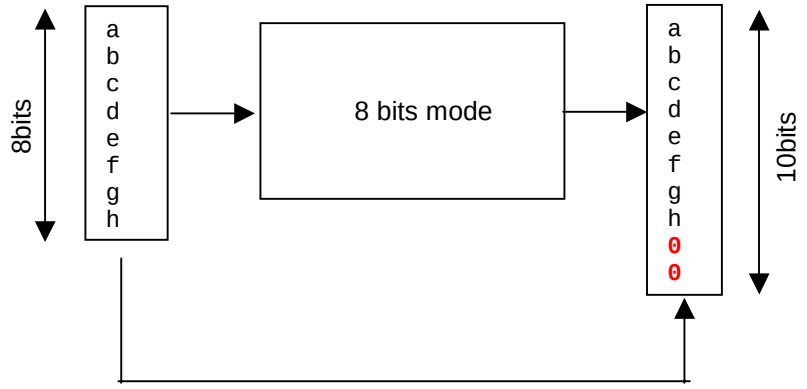


Figure 27: 8-bits mode

A-law Mode

In this mode each input raw data pixel has width of 8bits. The raw data stored in SDRAM as shown below

31 24	23 16	15 8	7 0
Pixel N+3	Pixel N+2	Pixel N+1	Pixel N

Internally preview engine always processes raw data with 10 bits per pixel. When processing the 8-bit raw data, the preview engine expands the data from 8 bits to 10 bits by using inverse A-law table as shown in Figure 28. Refer to ITU-T G.711 specification for A-law/Inverse A-law characteristics

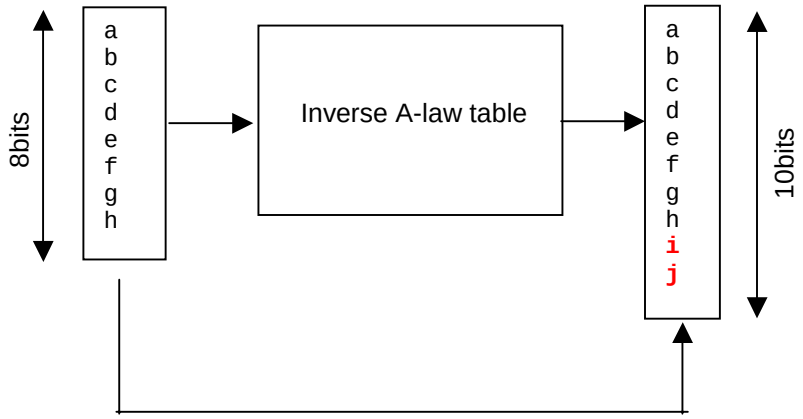


Figure 28: A-law mode

2.4.3 Defining Output Image Size

The size of the processed Preview Engine output image is determined by HSIZE,

VSIZE, HRSZ and VRSZ registers.

IMPORTANT: Up-sampling is only possible when operating in SDRAM mode, i.e. when bit INMODE of PVSET1 register is set to 1.

Depending on the values of the HRSZ and the VRSZ, the preview engine may send an extra burst (32-bytes) to SDRAM. It is recommended to have SDRAM work that is at least 32-bytes larger than the expected output image size.

Note: The maximum size of the number of lines output is 720 lines.

2.4.3.1 Burst Alignment

The Preview Engine always transfers data to the SDRC in bursts of 32-bytes. If BSTAL bit in PVSET1 register is cleared and the Preview Engine is configured such that number of horizontal pixels output (Hout) is not a multiple of 32-bytes (16 pixels), then the Preview Engine will transfer Hout in addition to some excess data in the final 32-byte transfer per horizontal line. It is recommended to reserve additional bytes of SDRAM for the excess data, in-order-to avoid unexpected overwriting of an important segment of SDRAM.

If BSTAL bit in PVSET1 register is set to 1 and the Preview Engine is configured such that Hout is a multiple of 32-bytes (16 pixels), the horizontal size of transferred data will be burst aligned, and excess pixel data will be discarded.

```
i.e, when  BSTAL=0,
if(Hresizeout % 16 != 0)
  Hout = Hresizeout + 16 -  Hresizeout % 16
else
  Hout = Hresizeout

and when BSTAL=1,  Hout = Hresizeout - (Hresizeout % 16)
```

where, Hout, is number of pixels per line output to SDRAM and Hreszieout, is number of pixels per line after resizing. Note that, 1 pixel = 16-bits.

2.4.3.2 Output Image Size Calculation

The size of the output image from the preview engine is determined by the HSIZE,
VSIZE, HRSZ and VRSZ registers as per the equations shown below.

$$H_{out} = \begin{cases} H\_SIZE \times \dfrac{64}{H\_RSZ} & (\text{if } H\_RSZ \geq 64) \\ (H\_SIZE - 1) \times \dfrac{64}{H\_RSZ} & (\text{if } H\_RSZ < 64) \end{cases}$$

$$V_{out} = V\_SIZE \times \frac{64}{V\_RSZ}$$

NOTE: When Preview Engine is configured to take input from SDRAM, the register HSTART must be set with the pixel width of input data present in the SDRAM as shown in Figure 29.

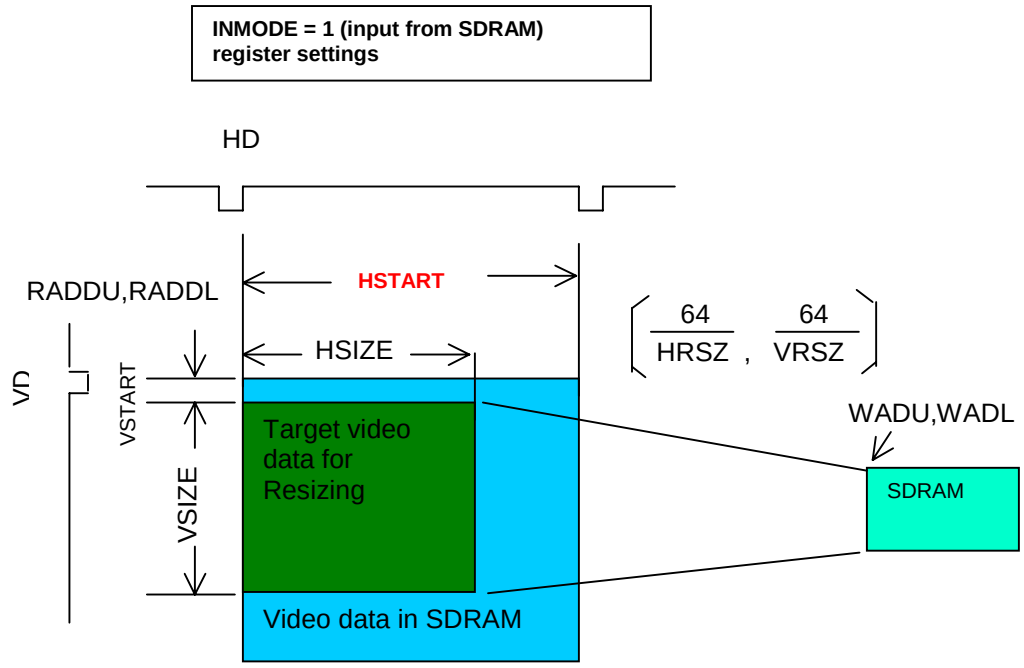


Figure 29: Preview Image parameters in SDRAM input mode

2.4.4 One-shot preview

When the PVOS bit in the PVSET1 register is set, the Preview Engine will process only one frame of data, and then automatically deactivate. Figure 30 shows signal timings in one-shot mode.

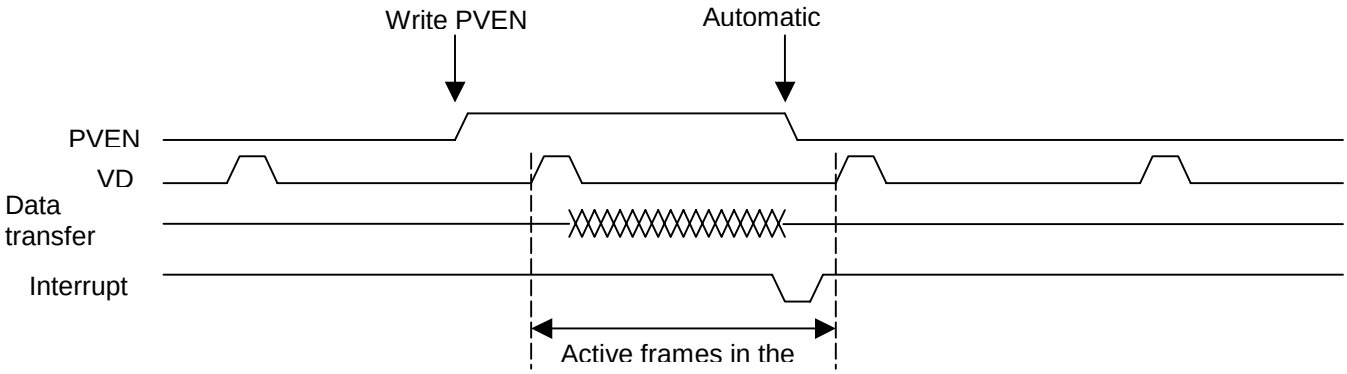


Figure 30: One-shot Mode Timings

2.4.5 Preview Engine Operation Examples

This section gives few examples on configuration and control of preview engine. Refer to “Appendix” for description about the CSL macro notation used in this section.

2.4.5.1 Example 1.

CCD input raw data size is 1536x240, 10-bits per pixel
Required Preview engine output size is 720x240
Preview Engine data output address is 0x97AB00

The sample code for this configuration is given in Figure 31

2.4.5.2 Example 2

SDRAM input raw data size is 1536x240, 10-bits per pixel
Required Preview engine output size is 720x480
Preview Engine data output address is 0x97AB00
Preview Engine data input address is 0xA7AB00
One-shot mode processing is required.

The sample code for this configuration is given in Figure 32

```
Uint16 input_width = 1536;
Uint16 input_height = 240;
Uint16 output_width = 720;
Uint16 output_height = 480;
Uint32 write_addr = 0x97Ab00;
Uint32 read_addr  = 0xA7Ab00;

PREV_RSET(PVEN, 0);                         // disable Preview Engine
while(PREV_RGET(PVEN));                     / wait till preview is disabled

PREV_FSET(PVSET1, 8BITS, 0 );               // 10 bits input mode
PREV_FSET(PVSET1, ALAW, 0);                 // Normal Mode
PREV_FSET(PVSET1, PVOS, 1);                 // Enable one-shot mode
PREV_FSET(PVSET1, RSONLY, 0);               / Normal Mode–raw CCD data
PREV_FSET(PVSET1, INMODDE, 1);              / SDRAM Input Mode
PREV_FSET(PVSET1, BSTAL, 1);                / burst align mode
PREV_FSET(PVSET1, WEN, 0);                  // ignore WEN signal

write_addr = (write_addr – 0x900000)/32;
PREV_RSET( WADRH, write_addr >> 16 );
PREV_RSET( WADRL, write_addr & 0xFFFF );

read_addr = (read_addr – 0x900000)/32;
PREV_RSET( RADRH, read_addr >> 16 );
PREV_RSET( RADRL, read_addr & 0xFFFF );
PREV_RSET( HSTART, input_width);            // horizontal size of data in SDRAM, units of pixels


PREV_RSET( VSTART, 0);                      // read data from 1st line in SDRAM

prev_hsize = input_width;
prev_vsize = input_height;

prev_hrsz  = ( prev_hsize * 16 ) / output_width;
prev_hsize = ( prev_hrsz * output_width) / 16;

// since for horizontal upscaling Hout = (HSIZE-1)*16/HRSZ
if(output_width > input_width )
    prev_hsize++;

prev_vrsz  = ( prev_vsize* 16 ) / output_height;
prev_vsize = ( prev_vrsz * output_height) / 16;

/*** Since 1536/720 = 2.13333 resize ratio is not supported by preview engine, only 1530 pixels are
taken as input so that (1530*16)/34 = 720 pixels will be output ***/

PREV_RSET( HSIZE, prev_hsize);              // HSIZE = 1530
PREV_RSET( HRSZ , prev_hrsz);               // HRSZ  = 34
PREV_RSET( VSIZE, prev_vsize);              // VSIZE = 240
PREV_RSET( VRSZ , prev_vrsz);               // VRSZ  = 8

// setup other registers depending on CCD raw data properties

PREV_RSET( SETUPY, 0x00FF); // no clipping of Y, C output data
PREV_RSET( SETUPC, 0x00FF);

PREV_RSET( PVEN, 1 ); // enable Preview Engine, start one shot mode

/*** wait for preview engine interrupt to indicate completion of one shot mode ***/
```

Figure 31: Sample code for Example 1

```
Uint16 input_width = 1536;
Uint16 input_height = 240;
Uint16 output_width = 720;
Uint16 output_height = 240;
Uint32 write_addr = 0x97Ab00;

PREV_RSET(PVEN, 0);                         // disable Preview Engine
while(PREV_RGET(PVEN))              // wait till preview is disabled   ;

PREV_FSET(PVSET1, 8BITS, 0 );               // 10 bits input mode
PREV_FSET(PVSET1, ALAW, 0);                 // Normal Mode
PREV_FSET(PVSET1, PVOS, 0);                 // Normal Mode–continuous
PREV_FSET(PVSET1, RSONLY, 0);       // Normal Mode–raw CCD data
PREV_FSET(PVSET1, INMODDE, 0);      // CCDC Input Mode
PREV_FSET(PVSET1, BSTAL, 1);        // burst align mode
PREV_FSET(PVSET1, WEN, 0);                  // ignore WEN signal

write_addr = (write_addr – 0x900000)/32;
PREV_RSET( WADRH, write_addr >> 16 );
PREV_RSET( WADRL, write_addr & 0xFFFF );

PREV_RSET( HSTART, . . .);          // depends on CCD module
PREV_RSET( VSTART, . . .);          // depends on CCD module

prev_hsize = input_width;
prev_vsize = input_height;

prev_hrsz  = ( prev_hsize * 16 )/output_width;
prev_hsize = ( prev_hrsz * output_width) / 16;

// since for horizontal upscaling Hout = (HSIZE-1)*16/HRSZ
if(output_width > input_width )
    prev_hsize++;

prev_vrsz  = ( prev_vsize* 16 ) / output_height;
prev_vsize = ( prev_vrsz * output_height) / 16;

/***Since 1536/720 = 2.13333 resize ratio is not supported by preview engine, only 1530 pixels are
taken as input so that (1530*16)/34 = 720 pixels will be output***/
PREV_RSET( HSIZE, prev_hsize);              // HSIZE = 1530
PREV_RSET( HRSZ , prev_hrsz);               // HRSZ  = 34
PREV_RSET( VSIZE, prev_vsize);              // VSIZE = 240
PREV_RSET( VRSZ , prev_vrsz);               // VRSZ  = 16

// setup other registers depending on CCD raw data properties

// no clipping of Y, C output data
PREV_RSET( SETUPY, 0x00FF);
PREV_RSET( SETUPC, 0x00FF);

PREV_RSET( PVEN, 1 );                       // enable Preview Engine
```

Figure 32: Sample code for Example 2

2.5 Fractional Notation

The fractional notation used in this chapter is as follows:

(S | U) x Q y

is used to denote a fractional numbers.
Here,
'x', represents the total number of bits in the real number including the fractional part
'y', represents the number of bits allocated to the fractional part. i.e **(x - y)** is the number of bits allocated to the integer part
'S', indicates that the number is signed, with negative numbers represented in 2's complement format
'U', indicates that the number is unsigned.

For example,
Precision: U10Q8

DGAIN[9:0]	Value
11 1111 1111	3.99609375 (3+255/256)
01 0000 0000	1.0
00 1000 0000	0.5
…	
00 0000 0001	0.00390625 (1/256)
00 0000 0000	0

U8Q5, means that the value can range from 0 to 7.96875
S8Q6, means that the value can range from –2 to 1.984375

2.6 Preview Engine Register Map (PREV)

Address	Register	Description
0003:0A80	PVEN	Preview Enable Register
0003:0A82	PVSET1	Preview Setup Register #1
0003:0A84	RADRH	SDRAM Read Address - high order bits
0003:0A86	RADRL	SDRAM Read Address - low order bits
0003:0A88	WADRH	SDRAM Write Address - high order bits
0003:0A8A	WADRL	SDRAM Write Address - low order bits
0003:0A8C	HSTART	Start pixel / Size horizontal
0003:0A8E	HSIZE	Number of pixels horizontal
0003:0A90	VSTART	Start line vertical
0003:0A92	VSIZE	Number of pixels vertical
0003:0A94	PVSET2	Preview Setup Register #2
0003:0A96	NFILT	Noise Filter Definition Register
0003:0A98	DGAIN	Digital Gain Register
0003:0A9A	WBGAIN0	White Balance Gain register #0
0003:0A9C	WBGAIN1	White Balance Gain register #1
0003:0A9E	SMTH	Smoothing Definition register
0003:0AA0	HRSZ	Horizontal Resize Register
0003:0AA2	VRSZ	Vertical Resize Register
0003:0AA4	BLOFST0	Black Level Offset Adjust #0
0003:0AA6	BLOFST1	Black Level Offset Adjust #1
0003:0AA8	MTXGAIN0	Matrix Gain register #0
0003:0AAA	MTXGAIN1	Matrix Gain register #1
0003:0AAC	MTXGAIN2	Matrix Gain register #2
0003:0AAE	MTXGAIN3	Matrix Gain register #3
0003:0AB0	MTXGAIN4	Matrix Gain register #4
0003:0AB2	MTXGAIN5	Matrix Gain register #5
0003:0AB4	MTXGAIN6	Matrix Gain register #6
0003:0AB6	MTXGAIN7	Matrix Gain register #7
0003:0AB8	MTXGAIN8	Matrix Gain register #8
0003:0ABA	MTXOFST0	R_offset register
0003:0ABC	MTXOFST1	G_offset register
0003:0ABE	MTXOFST2	B_offset register
0003:0AC0	GAMTBYP	GAMMA table bypass register
0003:0AC2	CSC0	Color Space Conversion Coefficient register #0
0003:0AC4	CSC1	Color Space Conversion Coefficient register #1
0003:0AC6	CSC2	Color Space Conversion Coefficient register #2
0003:0AC8	CSC3	Color Space Conversion Coefficient register #3
0003:0ACA	CSC4	Color Space Conversion Coefficient register #4
0003:0ACC	YOFST	Y offset register
0003:0ACE	COFST	Cb and Cr offset register
0003:0AD0	CNTBRT	Contrast and brightness adjustment register
0003:0AD2	CSUP0	Chroma Suppression Register #0
0003:0AD4	CSUP1	Chroma Suppression Register #1
0003:0AD6	SETUPY	Y max and min setup register
0003:0AD8	SETUPC	Cb and Cr max and min setup register
0003:0ADA	TABLE_ADDR	Address for Gamma table for luminance
0003:0ADC	TABLE_DATA	Data for Gamma table for luminance

0003:0ADE	HG_CTL	Histogram control
0003:0AE0	HG_R0_HSTART	Histogram Region 0 horizontal start location
0003:0AE2	HG_R0_HSIZE	Histogram Region 0 horizontal size
0003:0AE4	HG_R0_VSTART	Histogram Region 0 vertical start location
0003:0AE6	HG_R0_VSIZE	Histogram Region 0 vertical size
0003:0AE8	HG_R1_HSTART	Histogram Region 1 horizontal start location
0003:0AEA	HG_R1_HSIZE	Histogram Region 1 horizontal size
0003:0AEC	HG_R1_VSTART	Histogram Region 1 vertical start location
0003:0AEE	HG_R1_VSIZE	Histogram Region 1 vertical size
0003:0AF0	HG_R2_HSTART	Histogram Region 2 horizontal start location
0003:0AF2	HG_R2_HSIZE	Histogram Region 2 horizontal size
0003:0AF4	HG_R2_VSTART	Histogram Region 2 vertical start location
0003:0AF6	HG_R2_VSIZE	Histogram Region 2 vertical size
0003:0AF8	HG_R3_HSTART	Histogram Region 3 horizontal start location
0003:0AFA	HG_R3_HSIZE	Histogram Region 3 horizontal size
0003:0AFC	HG_R3_VSTART	Histogram Region 3 vertical start location
0003:0AFE	HG_R3_VSIZE	Histogram Region 3 vertical size
0003:0B00	HG_ADDR	Address for Histogram entry
0003:0B02	HG_DATA	Histogram data

2.7 Preview Engine Registers

2.7.1 PVEN

Preview Enable Register

PVEN 0003:0A80 offset: 0x00 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	PVEN
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

Bit	Name	Reset Value	R/W	Function
15:1	RSV			Reserved
0	PVEN	0	R/W	Preview Enable » 0: disable « » 1: enable « *Turns Preview Engine on or off* **This bit is latched by VD.*

2.7.2 PVSET1

Preview Setup Register #1

PVSET1 0003:0A82 offset: 0x02 default: 0x8080

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ATAWIDTH	ATAWIDTH	ATAWIDTH	INVD	SENSOR	SENSOR	SENSOR	SENSOR[1]	SENSOR[0]	PACK8	ALAW	PVOS	RSONLY	INMODE	BSTAL	WEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	DATAWIDTH	4	R/W	Preview data width » 0: 14 bit « » 1: 13 bit « » 2: 12 bit « » 3: 11 bit « » 4: 10 bit (default) « » 5: 9 bit « » 6: 8 bit « » 7: Reserved «
12	INVD	0	R/W	VD generated internally for one-shot preview » 0: No Internal VD « » 1: Internal VD generated «
11:7	SENSOR	1	R/W	Type of sensor » 00001: Bayer pattern sensor « » 00010: Sony VGA sensor « » 00100: Reserved « » 01000: Foveon sensor « » 10000: Reserved « Note: One bit of bit11/10/9/8/7 should set "1""
6	PACK8	0	R/W	Data storage in SDRAM » 0: 16-bit per pixel « » 1: 8-bit mode per pixel «
5	ALAW	0	R/W	Inverse A-LAW mode » 0: Normal mode « » 1: Inverse A-LAW mode « **This bit is latched by VD.*
4	PVOS	0	R/W	Preview One Shot » 0: normal (continuous processing) « » 1: one frame only «
3	RSONLY	0	R/W	Re-Size Only - Select type of input data » 0: Normal (raw CCD data) « » 1: Resizing only mode (YCbCr-4:2:2 data input) « **This bit is latched by VD.*
2	INMODE	0	R/W	Input Mode » 0: CCD Controller Interface « » 1: SDRAM Controller Interface «
1	BSTAL	0	R/W	Burst Aligned » 0: normal « » 1: burst aligned mode « *Apply a burst aligned transfer of output image to SDRAMC. If it is set to 1, the horizontal size is aligned to the burst length and surplus pixels are disregarded.*
0	WEN	0	R/W	Write Enable » 0: ignore « » 1: valid « *Select handling of a write enable signal from the CCDC. If set to 1 and the write enable signal is low, the preview engine is suspended in the frame.*

2.7.3 RADRH

SDRAM Read Address - high order bits

RADRH 0003:0A84 offset: 0x04 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADRH[6]	ADRH[5]	ADRH[4]	ADRH[3]	ADRH[2]	ADRH[1]	ADRH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	ADRH	0	R/W	Specifies upper 7 bits of the SDRAM source address used when INMODE in HSTART = '1'. Note: The address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*

2.7.4 RADRL

SDRAM Read Address - low order bits

RADRL 0003:0A86 offset: 0x06 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADRL[15]	ADRL[14]	ADRL[13]	ADRL[12]	ADRL[11]	ADRL[10]	ADRL[9]	ADRL[8]	ADRL[7]	ADRL[6]	ADRL[5]	ADRL[4]	ADRL[3]	ADRL[2]	ADRL[1]	ADRL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	ADRL	0	R/W	Specifies lower 16 bits of the SDRAM source address used when INMODE in HSTART = '1'. Note: The address is specified offset from the SDRAM base address in units of 32 bytes. *This bit is latched by VD.

2.7.5 WADRH

SDRAM Write Address - high order bits

WADRH 0003:0A88 offset: 0x08 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADRH[6]	ADRH[5]	ADRH[4]	ADRH[3]	ADRH[2]	ADRH[1]	ADRH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	ADRH	0	R/W	Specifies upper 7 bits of the SDRAM destination address for Preview Engine output data. Note: The address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*

2.7.6 WADRL

SDRAM Write Address - low order bits

WADRL 0003:0A8A offset: 0x0A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADRL[15]	ADRL[14]	ADRL[13]	ADRL[12]	ADRL[11]	ADRL[10]	ADRL[9]	ADRL[8]	ADRL[7]	ADRL[6]	ADRL[5]	ADRL[4]	ADRL[3]	ADRL[2]	ADRL[1]	ADRL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	ADRL	0	R/W	Specifies lower 16 bits of the SDRAM destination address for Preview Engine output data. Note: The address is specified offset from the SDRAM base address in units of 32 bytes. *This bit is latched by VD.

2.7.7 HSTART

Start pixel horizontal (for CCD input) or size in SDRAM (for SDRAM input)

HSTART 0003:0A8C offset: 0x0C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSTRT[11]	HSTRT[10]	HSTRT[9]	HSTRT[8]	HSTRT[7]	HSTRT[6]	HSTRT[5]	HSTRT[4]	HSTRT[3]	HSTRT[2]	HSTRT[1]	HSTRT[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSTRT	0	R/W	If INMODE=0: - Sets horizontal start position of valid input image If INMODE=1: - Sets horizontal size of input image in SDRAM *This bit is latched by VD.*

2.7.8 HSIZE

Number of pixels horizontal

HSIZE 0003:0A8E offset: 0x0E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSIZE[11]	HSIZE[10]	HSIZE[9]	HSIZE[8]	HSIZE[7]	HSIZE[6]	HSIZE[5]	HSIZE[4]	HSIZE[3]	HSIZE[2]	HSIZE[1]	HSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSIZE	0	R/W	Sets horizontal size of input image Note: The horizontal size of the output image must be lower than 720 pixels due to the size of implemented line memories. *This bit is latched by VD.

2.7.9 VSTART

Start line vertical

VSTART 0003:0A90 offset: 0x10 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSTRT[11]	VSTRT[10]	VSTRT[9]	VSTRT[8]	VSTRT[7]	VSTRT[6]	VSTRT[5]	VSTRT[4]	VSTRT[3]	VSTRT[2]	VSTRT[1]	VSTRT[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSTRT	0	R/W	Set vertical start position of a valid input image from the start of VD. **This bit is latched by VD.*

2.7.10 VSIZE

Number of pixels vertical

VSIZE 0003:0A92 offset: 0x12 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSIZE[11]	VSIZE[10]	VSIZE[9]	VSIZE[8]	VSIZE[7]	VSIZE[6]	VSIZE[5]	VSIZE[4]	VSIZE[3]	VSIZE[2]	VSIZE[1]	VSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSIZE	0	R/W	Set vertical size of a valid input image **This bit is latched by VD.*

2.7.11 PVSET2

Preview Setup Register #2

PVSET2 0003:0A94 offset: 0x14 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HINT	VINT	VNFILT	CCDMOD	VDNINT	GBLND[2]	GBLND[1]	GBLND[0]	EPEL[1]	EPEL[0]	OPEL[1]	OPEL[0]	EPOL[1]	EPOL[0]	OPOL[1]	OPOL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	HINT	0	R/W	Horizontal Process » 0: Other peripheral color information is used (5 types)« » 1: Same color information is used (2 types) «
14	VINT	0	R/W	Vertical Process » 0: Other peripheral color information is used (5 types)« » 1: Same color information is used (2 types) «
13	VNFILT	0	R/W	Vertical Noise Filter » 0: disable « » 1: enable «
12	CCDMOD	0	R/W	CCD Sensor Mode » 0: RGB color space « » 1: Complementary color space «
11	VDNINT	0	R/W	Interrupt every frame » 0: Generate Interrupt once when preview is OFF « » 1: Generate Interrupt every frame «
10:8	GBLND	0	R/W	Green Blend In complementary CCD mode, adjust blending ratio between original green and a calculated green from the other colors. Goutput = rGorg + (1-r)(Ye+Cy-Mg) » 000: r=1 « » 001: r=3/4 « » 010: r=1/2 « » 011: r=1/4 « » 100: r=0 «
7:6	EPEL	0	R/W	Color Pattern for Even Pixel, Even Line » 00: Gb/Ye « » 01: B/Cy « » 10: R/Mg « » 11: Gr/Gr «
5:4	OPEL	0	R/W	Color Pattern for Odd Pixel, Even Line » 00: Gb/Ye « » 01: B/Cy « » 10: R/Mg « » 11: Gr/Gr «
3:2	EPOL	0	R/W	Color Pattern for Even Pixel, Odd Line » 00: Gb/Ye « » 01: B/Cy « » 10: R/Mg « » 11: Gr/Gr «
1:0	OPOL	0	R/W	Color Pattern for Odd Pixel, Odd Line » 00: Gb/Ye « » 01: B/Cy « » 10: R/Mg « » 11: Gr/Gr «

2.7.12 NFILT

Noise Filter Definition Register

NFILT 0003:0A96 offset: 0x16 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THR[9]	THR[8]	THR[7]	THR[6]	THR[5]	THR[4]	THR[3]	THR[2]	THR[1]	THR[0]	RSV	NFEN	RSV	RSV	NFRT[1]	NFRT[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-	-	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	-	0	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:6	THR	0	R/W	Threshold value for the noise filter Precision is U10Q0
5	RSV			Reserved
4	NFEN	0	R/W	Horizontal Noise Filter Enable » 0: disable « » 1: enable «
3:2	RSV			Reserved
1:0	NFRT	0	R/W	Strength of Horizontal Noise Filter » 00: weak « » 01: a little weak « » 10: a little strong « » 11: strong «

2.7.13 DGAIN

Digital Gain Register

DGAIN 0003:0A98 offset: 0x18 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	DGAIN[9]	DGAIN[8]	DGAIN[7]	DGAIN[6]	DGAIN[5]	DGAIN[4]	DGAIN[3]	DGAIN[2]	DGAIN[1]	DGAIN[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	DGAIN	256	R/W	Digital Gain Value Precision is U10Q8, i.e. Decimal point is between 7 and 8 Range is 0-3.99609375

2.7.14 WBGAIN0

White Balance Gain register #0

WBGAIN0 0003:0A9A offset: 0x1A default: 0x2020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WG00[7]	WG00[6]	WG00[5]	WG00[4]	WG00[3]	WG00[2]	WG00[1]	WG00[0]	WG01[7]	WG01[6]	WG01[5]	WG01[4]	WG01[3]	WG01[2]	WG01[1]	WG01[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	WG00	32	R/W	White Balance Gain for Gb/Ye Precision is U8Q5, I.e. decimal point is between 4 and 5
7:0	WG01	32	R/W	White Balance Gain for B/Cy Precision is U8Q5, I.e. decimal point is between 4 and 5

2.7.15 WBGAIN1

White Balance Gain register #1

WBGAIN1 0003:0A9C offset: 0x1C default: 0x2020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WG02[7]	WG02[6]	WG02[5]	WG02[4]	WG02[3]	WG02[2]	WG02[1]	WG02[0]	WG03[7]	WG03[6]	WG03[5]	WG03[4]	WG03[3]	WG03[2]	WG03[1]	WG03[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	WG02	32	R/W	White Balance Gain for Gr/G Precision is U8Q5, I.e. decimal point is between 4 and 5
7:0	WG03	32	R/W	White Balance Gain for R/Mg Precision is U8Q5, I.e. decimal point is between 4 and 5

2.7.16 SMTH

Smoothing Definition register

SMTH 0003:0A9E offset: 0x1E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	SMEN	SMLVL
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:2	RSV			Reserved
1	SMEN	0	R/W	Enable smoothing function for processed image » 0: disable « » 1: enable «
0	SMLVL	0	R/W	Set smoothing level » 0: weak « » 1: strong «

2.7.17 HRSZ

Horizontal Resize Register

HRSZ 0003:0AA0 offset: 0x20 default: 0x0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HRSZD[11]	HRSZD[10]	HRSZD[9]	HRSZD[8]	HRSZD[7]	HRSZD[6]	HRSZD[5]	HRSZD[4]	HRSZD[3]	HRSZD[2]	HRSZD[1]	HRSZD[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HRSZD	64	R/W	Horizontal Resizing Parameter Horizontal Resize Ratio, R_H = 64/HRSZD Note: The horizontal size of the output image must be lower than 720 pixels due to the size of implemented line memories.

2.7.18 VRSZ

Vertical Resize Register

VRSZ 0003:0AA2 offset: 0x22 default: 0x0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VRSZD[11]	VRSZD[10]	VRSZD[9]	VRSZD[8]	VRSZD[7]	VRSZD[6]	VRSZD[5]	VRSZD[4]	VRSZD[3]	VRSZD[2]	VRSZD[1]	VRSZD[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VRSZD	64	R/W	Vertical Resizing Parameter Vertical Resize Ratio, V_H = 64/VRSZD

2.7.19 BLOFST0

Black Level Offset Adjust #0

BLOFST0 0003:0AA4 offset: 0x24 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLR[7]	BLR[6]	BLR[5]	BLR[4]	BLR[3]	BLR[2]	BLR[1]	BLR[0]	BLG[7]	BLG[6]	BLG[5]	BLG[4]	BLG[3]	BLG[2]	BLG[1]	BLG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	BLR	0	R/W	Black level offset adjustment for R. BLR in 2's complement format
7:0	BLG	0	R/W	Black level offset adjustment for G. BLG is in 2's complement format

2.7.20 BLOFST1

Black Level Offset Adjust #1

BLOFST1 0003:0AA6 offset: 0x26 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLB[7]	BLB[6]	BLB[5]	BLB[4]	BLB[3]	BLB[2]	BLB[1]	BLB[0]	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Bit	Name	Reset Value	R/W	Function
15:8	BLB	0	R/W	Black level offset adjustment for B. BLB in 2's complement format
7:0	RSV			Reserved

2.7.21 MTXGAIN0

Matrix Gain register #0

MTXGAIN0 0003:0AA8 offset: 0x28 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXRR[11]	MTXRR[10]	MTXRR[9]	MTXRR[8]	MTXRR[7]	MTXRR[6]	MTXRR[5]	MTXRR[4]	MTXRR[3]	MTXRR[2]	MTXRR[1]	MTXRR[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXRR	256	R/W	MTX_RR value of RGB2RGB matrix R_{out} = |MTXRR MTXGR MTXBR | |R_{in}| |MXR| G_{out} = |MTXRG MTXGG MTXBG | x |G_{in}| + |MXG| B_{out} = |MTXRB MTXGB MTXBB | |B_{in}| |MXB|

2.7.22 MTXGAIN1

Matrix Gain register #1

MTXGAIN1 0003:0AAA offset: 0x2A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXGR[11]	MTXGR[10]	MTXGR[9]	MTXGR[8]	MTXGR[7]	MTXGR[6]	MTXGR[5]	MTXGR[4]	MTXGR[3]	MTXGR[2]	MTXGR[1]	MTXGR[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXGR	0	R/W	MTX_GR value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.23 MTXGAIN2

Matrix Gain register #2

MTXGAIN2 0003:0AAC offset: 0x2C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXBR[11]	MTXBR[10]	MTXBR[9]	MTXBR[8]	MTXBR[7]	MTXBR[6]	MTXBR[5]	MTXBR[4]	MTXBR[3]	MTXBR[2]	MTXBR[1]	MTXBR[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXBR	0	R/W	MTX_BR value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.24 MTXGAIN3

Matrix Gain register #3

MTXGAIN3 0003:0AAE offset: 0x2E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXRG[11]	MTXRG[10]	MTXRG[9]	MTXRG[8]	MTXRG[7]	MTXRG[6]	MTXRG[5]	MTXRG[4]	MTXRG[3]	MTXRG[2]	MTXRG[1]	MTXRG[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXRG	0	R/W	MTX_RG value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.25 MTXGAIN4

Matrix Gain register #4

MTXGAIN4 0003:0AB0 offset: 0x30 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXGG[11]	MTXGG[10]	MTXGG[9]	MTXGG[8]	MTXGG[7]	MTXGG[6]	MTXGG[5]	MTXGG[4]	MTXGG[3]	MTXGG[2]	MTXGG[1]	MTXGG[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXGG	256	R/W	MTX_GG value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.26 MTXGAIN5

Matrix Gain register #5

MTXGAIN5 0003:0AB2 offset: 0x32 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXBG[11]	MTXBG[10]	MTXBG[9]	MTXBG[8]	MTXBG[7]	MTXBG[6]	MTXBG[5]	MTXBG[4]	MTXBG[3]	MTXBG[2]	MTXBG[1]	MTXBG[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXBG	0	R/W	MTX_BG value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.27 MTXGAIN6

Matrix Gain register #6

MTXGAIN6 0003:0AB4 offset: 0x34 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXRB[11]	MTXRB[10]	MTXRB[9]	MTXRB[8]	MTXRB[7]	MTXRB[6]	MTXRB[5]	MTXRB[4]	MTXRB[3]	MTXRB[2]	MTXRB[1]	MTXRB[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXRB	0	R/W	MTX_RB value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.28 MTXGAIN7

Matrix Gain register #7

MTXGAIN7 0003:0AB6 offset: 0x36 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXGB[11]	MTXGB[10]	MTXGB[9]	MTXGB[8]	MTXGB[7]	MTXGB[6]	MTXGB[5]	MTXGB[4]	MTXGB[3]	MTXGB[2]	MTXGB[1]	MTXGB[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXGB	0	R/W	MTX_GB value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.29 MTXGAIN8

Matrix Gain register #8

MTXGAIN8 0003:0AB8 offset: 0x38 default: 0x0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	MTXBB[11]	MTXBB[10]	MTXBB[9]	MTXBB[8]	MTXBB[7]	MTXBB[6]	MTXBB[5]	MTXBB[4]	MTXBB[3]	MTXBB[2]	MTXBB[1]	MTXBB[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	MTXBB	256	R/W	MTX_BB value of RGB2RGB matrix Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.30 MTXOFST0

R_offset register

MTXOFST0 0003:0ABA offset: 0x3A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	MXR[9]	MXR[8]	MXR[7]	MXR[6]	MXR[5]	MXR[4]	MXR[3]	MXR[2]	MXR[1]	MXR[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	MXR	0	R/W	R_offset used in the RGB2RGB matrix conversion MXR is in 2's complement format. Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.31 MTXOFST1

G_offset register

MTXOFST1 0003:0ABC offset: 0x3C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	MXG[9]	MXG[8]	MXG[7]	MXG[6]	MXG[5]	MXG[4]	MXG[3]	MXG[2]	MXG[1]	MXG[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	MXG	0	R/W	G_offset used in the RGB2RGB matrix conversion MXG is in 2's complement format. Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.32 MTXOFST2

B_offset register

MTXOFST2 0003:0ABE offset: 0x3E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	MXB[9]	MXB[8]	MXB[7]	MXB[6]	MXB[5]	MXB[4]	MXB[3]	MXB[2]	MXB[1]	MXB[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	MXB	0	R/W	B_offset used in the RGB2RGB matrix conversion MXB is in 2's complement format. Note: Refer MTXGAIN0 for the RGB-RGB matrix equation

2.7.33 GAMTSBYP

GAMMA table bypass register

GAMTBYP 0003:0AC0 offset: 0x40 default: 0x0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ROM	RSV	BYPR	BYPG	BYPB
R/W	-	-	-	-	-	-	-	-	-	-	-	R/W	-	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	1	-	0	0	0

Bit	Name	Reset Value	R/W	Function
15:5	RSV			Reserved
4	ROM	1	R/W	Gamma ROM Table Select » 0: Piece-wise linear RAM table « » 1: ROM Table «
3	RSV			Reserved
2	BYPR	0	R/W	Gamma RAM Table Bypass for Red » 0: Use RAM gamma table for R « » 1: Bypass gamma table for R «
1	BYPG	0	R/W	Gamma RAM Table Bypass for Green » 0: Use RAM gamma table for G « » 1: Bypass gamma table for G «
0	BYPB	0	R/W	Gamma RAM Table Bypass for Blue » 0: Use RAM gamma table for B « » 1: Bypass gamma table for B «

2.7.34 CSC0

Color Space Conversion Coefficient register #0

CSC0 0003:0AC2 offset: 0x42 default: 0x1326

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSCRY[7]	CSCRY[6]	CSCRY[5]	CSCRY[4]	CSCRY[3]	CSCRY[2]	CSCRY[1]	CSCRY[0]	CSCGY[7]	CSCGY[6]	CSCGY[5]	CSCGY[4]	CSCGY[3]	CSCGY[2]	CSCGY[1]	CSCGY[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0

Bit	Name	Reset Value	R/W	Function
15:8	CSCRY	19	R/W	Color Space Conversion Coefficient of R for computing Y Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format
7:0	CSCGY	38	R/W	Color Space Conversion Coefficient of G for computing Y Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format

2.7.35 CSC1

Color Space Conversion Coefficient register #1

CSC1 0003:0AC4 offset: 0x44 default: 0x07F5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSCBY[7]	CSCBY[6]	CSCBY[5]	CSCBY[4]	CSCBY[3]	CSCBY[2]	CSCBY[1]	CSCBY[0]	CSCRCB[7]	CSCRCB[6]	CSCRCB[5]	CSCRCB[4]	CSCRCB[3]	CSCRCB[2]	CSCRCB[1]	CSCRCB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1

Bit	Name	Reset Value	R/W	Function
15:8	CSCBY	7	R/W	Color Space Conversion Coefficient of B for computing Y Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format
7:0	CSCRCB	245	R/W	Color Space Conversion Coefficient of R for computing Cb Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format

2.7.36 CSC2

Color Space Conversion Coefficient register #2

CSC2 0003:0AC6 offset: 0x46 default: 0xEB20

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSCGCB[7]	CSCGCB[6]	CSCGCB[5]	CSCGCB[4]	CSCGCB[3]	CSCGCB[2]	CSCGCB[1]	CSCGCB[0]	CSCBCB[7]	CSCBCB[6]	CSCBCB[5]	CSCBCB[4]	CSCBCB[3]	CSCBCB[2]	CSCBCB[1]	CSCBCB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	0	1	0	1	1	0	0	1	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	CSCGCB	235	R/W	Color Space Conversion Coefficient of G for computing Cb Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format
7:0	CSCBCB	32	R/W	Color Space Conversion Coefficient of B for computing Cb Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format

2.7.37 CSC3

Color Space Conversion Coefficient register #3

CSC3 0003:0AC8 offset: 0x48 default: 0x20E5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSCRCR[7]	CSCRCR[6]	CSCRCR[5]	CSCRCR[4]	CSCRCR[3]	CSCRCR[2]	CSCRCR[1]	CSCRCR[0]	CSCGCR[7]	CSCGCR[6]	CSCGCR[5]	CSCGCR[4]	CSCGCR[3]	CSCGCR[2]	CSCGCR[1]	CSCGCR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0	1	1	1	0	0	1	0	1

Bit	Name	Reset Value	R/W	Function
15:8	CSCRCR	32	R/W	Color Space Conversion Coefficient of R for computing Cr Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format
7:0	CSCGCR	229	R/W	Color Space Conversion Coefficient of G for computing Cr Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format

2.7.38 CSC4

Color Space Conversion Coefficient register #4

CSC4 0003:0ACA offset: 0x4A default: 0xFB00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSCBCR[7]	CSCBCR[6]	CSCBCR[5]	CSCBCR[4]	CSCBCR[3]	CSCBCR[2]	CSCBCR[1]	CSCBCR[0]	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-	-	-	-	-	-	-
Default	1	1	1	1	1	0	1	1	-	-	-	-	-	-	-	-

Bit	Name	Reset Value	R/W	Function
15:8	CSCBCR	251	R/W	Color Space Conversion Coefficient of B for computing Cr Precision is S8Q6, I.e., GAIN/(2^6), where GAIN is in 2's complement format
7:0	RSV			Reserved

2.7.39 YOFST

Y offset register

YOFST 0003:0ACC offset: 0x4C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	YOFST[7]	YOFST[6]	YOFST[5]	YOFST[4]	YOFST[3]	YOFST[2]	YOFST[1]	YOFST[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	YOFST	0	R/W	DC Offset value for Y (S8Q7) Yout = Yin + YOFST (-128:+127)

2.7.40 COFST

Cr and Cb offset register

COFST 0003:0ACE offset: 0x4E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFSTCB[7]	OFSTCB[6]	OFSTCB[5]	OFSTCB[4]	OFSTCB[3]	OFSTCB[2]	OFSTCB[1]	OFSTCB[0]	OFSTCR[7]	OFSTCR[6]	OFSTCR[5]	OFSTCR[4]	OFSTCR[3]	OFSTCR[2]	OFSTCR[1]	OFSTCR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	OFSTCB	0	R/W	DC Offset value for Cb (S8Q7) Cout = Cin + OFSTCB (-128:127)
7:0	OFSTCR	0	R/W	DC Offset value for Cr (S8Q7) Cout = Cin + OFSTCR (-128:127)

2.7.41 CNTBRT

Contrast and brightness adjustment register

CNTBRT 0003:0AD0 offset: 0x50 default: 0x1000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT[7]	CNT[6]	CNT[5]	CNT[4]	CNT[3]	CNT[2]	CNT[1]	CNT[0]	BRT[7]	BRT[6]	BRT[5]	BRT[4]	BRT[3]	BRT[2]	BRT[1]	BRT[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	CNT	16	R/W	Contrast Adjustment Sets the contrast of the Y data. Precision is U8Q4, x0 to x15 Applied after offset adjustments.
7:0	BRT	0	R/W	Bightness Adjustment Sets the brightness of Y data (0 to 255). Applied after contrast adjustments.

2.7.42 CSUP0

Chroma suppression register #0

CSUP0 0003:0AD2 offset: 0x52 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	YENHEN	CSUPEN
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:2	RSV			Reserved
1	YENHEN	0	R/W	Apply a non-linear luma enhancer function » 0: disable « » 1: enable «
0	CSUPEN	0	R/W	Apply a chroma suppression function » 0: disable « » 1: enable «

2.7.43 CSUP1

Chroma suppression register #1

CSUP1 0003:0AD4 offset: 0x54 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSUPTH[7]	CSUPTH[6]	CSUPTH[5]	CSUPTH[4]	CSUPTH[3]	CSUPTH[2]	CSUPTH[1]	CSUPTH[0]	CSUPG[7]	CSUPG[6]	CSUPG[5]	CSUPG[4]	CSUPG[3]	CSUPG[2]	CSUPG[1]	CSUPG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	CSUPTH	0	R/W	Chroma Supression Threshold
7:0	CSUPG	0	R/W	Gain value for Chroma Supression Function Precision is U8Q8 i.e (0 to 0.99609375)

2.7.44 SETUPY

Y max and min setup register

SETUPY 0003:0AD6 offset: 0x56 default: 0xFF00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAXY[7]	MAXY[6]	MAXY[5]	MAXY[4]	MAXY[3]	MAXY[2]	MAXY[1]	MAXY[0]	MINY[7]	MINY[6]	MINY[5]	MINY[4]	MINY[3]	MINY[2]	MINY[1]	MINY[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	MAXY	255	R/W	Maximum Y value, values greater than set value are clipped to the set value *Note: MAXY must be set for all modes of operation of the Preview Engine, which includes raw data input from CCD, raw data input from SDRAM, YUV resize only mode, one-shot mode.*
7:0	MINY	0	R/W	Minimum Y value. Values less than set value are clipped to the set value *Note: MINY must be set for all modes of operation of the Preview Engine, which includes raw data input from CCD, raw data input from SDRAM, YUV resize only mode, one-shot mode.*

2.7.45 SETUPC

Cb and Cr max and min setup register

SETUPC 0003:0AD8 offset: 0x58 default: 0xFF00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAXC[7]	MAXC[6]	MAXC[5]	MAXC[4]	MAXC[3]	MAXC[2]	MAXC[1]	MAXC[0]	MINC[7]	MINC[6]	MINC[5]	MINC[4]	MINC[3]	MINC[2]	MINC[1]	MINC[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	MAXC	255	R/W	Maximum Cb and Cr value, values greater than set value are clipped to the set value *Note: MAXC must be set for all modes of operation of the Preview Engine, which includes raw data input from CCD, raw data input from SDRAM, YUV resize only mode, one-shot mode.*
7:0	MINC	0	R/W	Minimum Cb and Cr value. Values less than set value are clipped to the set value *Note: MINC must be set for all modes of operation of the Preview Engine, which includes raw data input from CCD, raw data input from SDRAM, YUV resize only mode, one-shot mode.*

2.7.46 TABLE_ADDR

Address for Gamma table and non-linear Y table

TABLE_ADDR 0003:0ADA offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	ADDR[9]	ADDR[8]	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	ADDR	0	R/W	Address of gamma table and non linear Y enhancing table Note: The address is auto incremented after every read / write in the TABLE_DATA register

2.7.47 TABLE_DATA

Data for Gamma table and non-linear Y table

TABLE_DATA 0003:0ADC offset: 0x5C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	DATA[9]	DATA[8]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	DATA	0	R/W	Data of gamma table and non linear Y enhancing table Note: The data is copied to the location pointed by GAMMA_ADDR register. The address is auto incremented after every read / write in the TABLE_DATA register.

2.7.48 HG_CONTROL

Histogram control

HG_CTL 0003:0ADE offset: 0x5E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	CLR	ALWAYS	INT_ENB	CFA	BINS[1]	BINS[0]	RGN_ENB[1]	RGN_ENB[0]	SHIFT[2]	SHIFT[1]	SHIFT[0]	START_BUS
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11	CLR	0	R/W	Clear Data after read » 0: Enable clear when read « » 1: Disable clear when read «
10	ALWAYS	0	R/W	Histogram always On » 0: Disable (Start oneshot by writing 1 to START_BUSY) « » 1: Enable (Re-start automatically at beginning of each preview frame) «
9	INT_ENB	0	R/W	Interrupt enable » 0: Disable interrupt « » 1: Enable interrupt «
8	CFA	0	R/W	CFA pattern » 0: 2D (2 x 2) conventional patter « » 1: reserved «
7:6	BINS	0	R/W	No of bins per histogram » 0: 32 bins « » 1: 64 bins « » 2: 128 bins « » 3: 256 bins «
5:4	RGN_ENB	0	R/W	Number of regions enabled
3:1	SHIFT	0	R/W	No of bits to right shift data before accessing bins (0-7)
0	START_BUSY	0	R/W	Write When ALWAYS = 0, 1 to start histogram calculation Read 1 - Calculation under progress 0 - Calculation is done

2.7.49 HG_R0_HSTART

Histogram region 0 horizontal start location

HG_R0_HSTART 0003:0AE0 offset: 0x60 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSTART[11]	HSTART[10]	HSTART[9]	HSTART[8]	HSTART[7]	HSTART[6]	HSTART[5]	HSTART[4]	HSTART[3]	HSTART[2]	HSTART[1]	HSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSTART	0	R/W	Horizontal start location for region 0

2.7.50 HG_R0_HSIZE

Histogram region 0 horizontal size

HG_R0_HSIZE 0003:0AE2 offset: 0x62 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSIZE[11]	HSIZE[10]	HSIZE[9]	HSIZE[8]	HSIZE[7]	HSIZE[6]	HSIZE[5]	HSIZE[4]	HSIZE[3]	HSIZE[2]	HSIZE[1]	HSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSIZE	0	R/W	Horizontal size for region 0

2.7.51 HG_R0_VSTART

Histogram region 0 Vertical start location

HG_R0_VSTART 0003:0AE4 offset: 0x64 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSTART[11]	VSTART[10]	VSTART[9]	VSTART[8]	VSTART[7]	VSTART[6]	VSTART[5]	VSTART[4]	VSTART[3]	VSTART[2]	VSTART[1]	VSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSTART	0	R/W	Vertical start location for region 0

2.7.52 HG_R0_VSIZE

Histogram region 0 vertical size

HG_R0_VSIZE 0003:0AE6 offset: 0x66 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSIZE[11]	VSIZE[10]	VSIZE[9]	VSIZE[8]	VSIZE[7]	VSIZE[6]	VSIZE[5]	VSIZE[4]	VSIZE[3]	VSIZE[2]	VSIZE[1]	VSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSIZE	0	R/W	Vertical size for region 0

2.7.53 HG_R1_HSTART

Histogram region 1 horizontal start location

HG_R1_HSTART 0003:0AE8 offset: 0x68 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSTART[11]	HSTART[10]	HSTART[9]	HSTART[8]	HSTART[7]	HSTART[6]	HSTART[5]	HSTART[4]	HSTART[3]	HSTART[2]	HSTART[1]	HSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSTART	0	R/W	Horizontal start location for region 1

2.7.54 HG_R1_HSIZE

Histogram region 1 horizontal size

HG_R1_HSIZE 0003:0AEA offset: 0x6A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSIZE[11]	HSIZE[10]	HSIZE[9]	HSIZE[8]	HSIZE[7]	HSIZE[6]	HSIZE[5]	HSIZE[4]	HSIZE[3]	HSIZE[2]	HSIZE[1]	HSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSIZE	0	R/W	Horizontal size for region 1

2.7.55 HG_R1_VSTART

Histogram region 1 Vertical start location

HG_R1_VSTART 0003:0AEC offset: 0x6C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSTART[11]	VSTART[10]	VSTART[9]	VSTART[8]	VSTART[7]	VSTART[6]	VSTART[5]	VSTART[4]	VSTART[3]	VSTART[2]	VSTART[1]	VSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSTART	0	R/W	Vertical start location for region 1

2.7.56 HG_R1_VSIZE

Histogram region 1 vertical size

HG_R1_VSIZE 0003:0AEE offset: 0x6E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSIZE[11]	VSIZE[10]	VSIZE[9]	VSIZE[8]	VSIZE[7]	VSIZE[6]	VSIZE[5]	VSIZE[4]	VSIZE[3]	VSIZE[2]	VSIZE[1]	VSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSIZE	0	R/W	Vertical size for region 1

2.7.57 HG_R2_HSTART

Histogram region 2 horizontal start location

HG_R2_HSTART 0003:0AF0 offset: 0x70 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSTART[11]	HSTART[10]	HSTART[9]	HSTART[8]	HSTART[7]	HSTART[6]	HSTART[5]	HSTART[4]	HSTART[3]	HSTART[2]	HSTART[1]	HSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSTART	0	R/W	Horizontal start location for region 2

2.7.58 HG_R2_HSIZE

Histogram region 2 horizontal size

HG_R2_HSIZE 0003:0AF2 offset: 0x72 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSIZE[11]	HSIZE[10]	HSIZE[9]	HSIZE[8]	HSIZE[7]	HSIZE[6]	HSIZE[5]	HSIZE[4]	HSIZE[3]	HSIZE[2]	HSIZE[1]	HSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSIZE	0	R/W	Horizontal size for region 2

2.7.59 HG_R2_VSTART

Histogram region 2 Vertical start location

HG_R2_VSTART 0003:0AF4 offset: 0x74 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSTART[11]	VSTART[10]	VSTART[9]	VSTART[8]	VSTART[7]	VSTART[6]	VSTART[5]	VSTART[4]	VSTART[3]	VSTART[2]	VSTART[1]	VSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSTART	0	R/W	Vertical start location for region 2

2.7.60 HG_R2_VSIZE

Histogram region 2 vertical size

HG_R2_VSIZE 0003:0AF6 offset: 0x76 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSIZE[11]	VSIZE[10]	VSIZE[9]	VSIZE[8]	VSIZE[7]	VSIZE[6]	VSIZE[5]	VSIZE[4]	VSIZE[3]	VSIZE[2]	VSIZE[1]	VSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSIZE	0	R/W	Vertical size for region 2

2.7.61 HG_R3_HSTART

Histogram region 3 horizontal start location

HG_R3_HSTART 0003:0AF8 offset: 0x78 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSTART[11]	HSTART[10]	HSTART[9]	HSTART[8]	HSTART[7]	HSTART[6]	HSTART[5]	HSTART[4]	HSTART[3]	HSTART[2]	HSTART[1]	HSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSTART	0	R/W	Horizontal start location for region 3

2.7.62 HG_R3_HSIZE

Histogram region 3 horizontal size

HG_R3_HSIZE 0003:0AFA offset: 0x7A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	HSIZE[11]	HSIZE[10]	HSIZE[9]	HSIZE[8]	HSIZE[7]	HSIZE[6]	HSIZE[5]	HSIZE[4]	HSIZE[3]	HSIZE[2]	HSIZE[1]	HSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	HSIZE	0	R/W	Horizontal size for region 3

2.7.63 HG_R3_VSTART

Histogram region 3 Vertical start location

HG_R3_VSTART 0003:0AFC offset: 0x7C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSTART[11]	VSTART[10]	VSTART[9]	VSTART[8]	VSTART[7]	VSTART[6]	VSTART[5]	VSTART[4]	VSTART[3]	VSTART[2]	VSTART[1]	VSTART[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSTART	0	R/W	Vertical start location for region 3

2.7.64 HG_R3_VSIZE

Histogram region 3 vertical size

HG_R3_VSIZE 0003:0AFE offset: 0x7E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	VSIZE[11]	VSIZE[10]	VSIZE[9]	VSIZE[8]	VSIZE[7]	VSIZE[6]	VSIZE[5]	VSIZE[4]	VSIZE[3]	VSIZE[2]	VSIZE[1]	VSIZE[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	VSIZE	0	R/W	Vertical size for region 3

2.7.65 HG_ADDR

Address for Histogram entry

HG_ADDR 0003:0B00 offset: 0x80 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	ADDR[10]	ADDR[9]	ADDR[8]	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	ADDR	0	R/W	Address for reading histogram entry

2.7.66 HG_DATA

Histogram data

HG_DATA 0003:0B02 offset: 0x82 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA[15]	DATA[14]	DATA[13]	DATA[12]	DATA[11]	DATA[10]	DATA[9]	DATA[8]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DATA	0	R/W	Histogram data

3 Hardware 3A

3.1 Introduction

DM320 provides real-time 3A (Auto Exposure / Auto White Balance / Auto Focus) statistics function. ARM can use these statistics to compute the optimal 3A control parameters.

AE/AWB statistics is calculated by using up to 96 windows. The windows are of the same size and organized as an m-by-n matrix. The organization of the matrix, the size of the windows and the method of calculation are user-selectable.

AF statistics is calculated by using up to 96 windows. The position and the size of each window can be independently configured.

3.2 Features

Auto Exposure / Auto White Balance:

96 windows organized as m-by-n matrix.

Number of windows in horizontal direction is between 1 – 12 and in vertical direction is between 1 - 8

Total number of pixels per window in horizontal direction is between 2 – 256 and in vertical direction is between 4 - 128

Sampling step for calculation in horizontal and vertical direction is between 2 - 32. Total number of 2x2 blocks in a window is up to 256

Outputs for each window are the accumulated R, Gr, Gb and B. The results are 16-bit integers stored in SDRAM readable by ARM

Auto Focus:

Total number of windows is up to 96 and is organized as a m-by-n matrix

The AF calculation can be performed only on green pixel data in the window

Two biquad filters are used to filter the green or Y pixel data. The coefficients of both filters are 10-bit wide and can be set by software

Number of windows in horizontal direction is between 1 – 12 and in vertical direction is between 1 - 8

Total number of green pixels per window in horizontal direction is between 1 - 256 and in vertical direction is between 2 -128

Figure 33 shows the block diagram of Hardware 3A module in DM320.

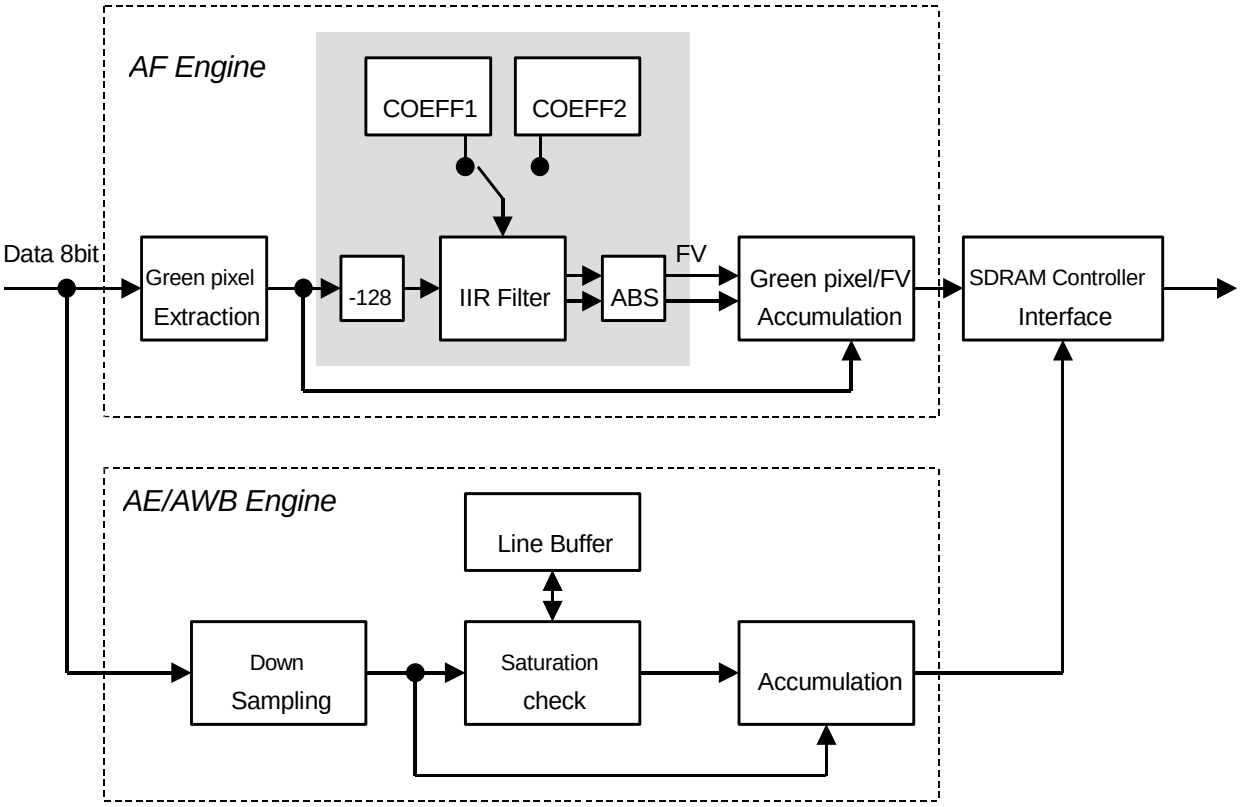


Figure 33 Block Diagram of 3A Hardware Engine

3.3 Input data for H3A Engine

The input signal to H3A engine is 8bit data selected with GWDI[2:0] of the CGAMMAWD register in CCDC.

Note: GWDI [2:0] selects 10-bit raw data, the higher 8-bits are taken as input by the H3A engine.

3.4 Auto Focus (AF) Engine

The input data to AF engine is the raw data output by the CCD Controller. The AF Engine extracts green pixel data from this raw data. The extracted green data are subtracted by 128, and fed to the filter block to calculate the Focus Value (FV), which is the absolute value of the IIR filter output. The maximum FV of each line in a Paxel is acquired if FV mode is set to 'Peak mode'. Value of the green pixels and either the FV or the maximum FV (of each line) are accumulated in the Paxel, and are stored in SDRAM.

The window configuration of the AF Engine is based on a frame formed by the extracted green pixels. Figure 34 illustrates the paxel configuration for AF engine. Table 15 illustrates the register fields used to configure AF Engine.

NOTE**:** Paxel in AF statistics is a window of green pixel data

Register Field	width	Description
AFEN (H3ACTRL)	1	AF Engine enable 0:disable 1:enable
GPOS(AFCTRL)	4	Green pixel position in 2x2 block Support 5/6/9/A and 1/2/4/8
PAXH (AFPAX1)	8	Paxel Width (PAXH+1) (1 – 256)
PAXV (AFPAX1)	7	Paxel Height (PAXV+1) (2 – 128)
PAXHC (AFPAX2)	4	Paxel Count for H direction (PAXHC+1) (1 – 12)
PAXVC(AFPAX2)	3	Paxel Count for V direction (PAXVC+1) (1 – 8)
PAXSH (AFPAX3)	12	Paxel start position (H) (1 – 4,095)
PAXSV (AFPAX4)	12	Paxel start position (V) (0 – 4,095)
IIRSH (AFIIRSH)	12	IIR filter start position (H) (0 – 4,095)
AFINCV(AFPAX5)	4	Line increments in a Paxel (AFINCV+1) (1-16)
FVMODE(AFCTRL)	1	Focus Value accumulation mode 0:Sum mode 1:Peak mode
COEFF1 (AFCOEFF10 to AFCOEFF110)	11x11	Coefficient table1 for IIR filter (decimal 6bit)
COEFF2 (AFCOEFF20 to AFCOEFF210)	11x11	Coefficient table2 for IIR filter (decimal 6bit)
AFSDRA (AFSDRA1, AFSDRA2)	23	SDRAM destination address to store the results of AF engine. It is automatically incremented until the two continuous buffers for the two successive frames become full.
AFSDRFLG (AFSDRFLG)	1	SDRAM buffer flag to indicate the buffer at which the results are stored.
AFERRFR(AFSDRFLG)	2	SDRAM access fail flag on previous buffer flag [0/1].
AFERR(AFSDRFLG)	1	SDRAM access fail flag. Clear by ARM write only.

Table 15: AF Engine Configuration Registers

Constraints for configuration of Auto focus engine are given below.

- PAXSH must be equal to or greater than (IIRSH + 1).
- Paxels cannot overlap the last pixel in a line. PAXSH, PAXH and PAXHC must be set accordingly.
- Paxels can overlap either the first or the last line in a frame, but not both of them. PAXSV, PAXV and PAXVC must be set accordingly.
- GPOS cannot pick continuous 2 data in a line. DM320 support 1/2/4/5/6/8/9/A values.
- PAXV=0 is NG. PAXH=0(or small value) might be problem in data transfer to SDRAM.

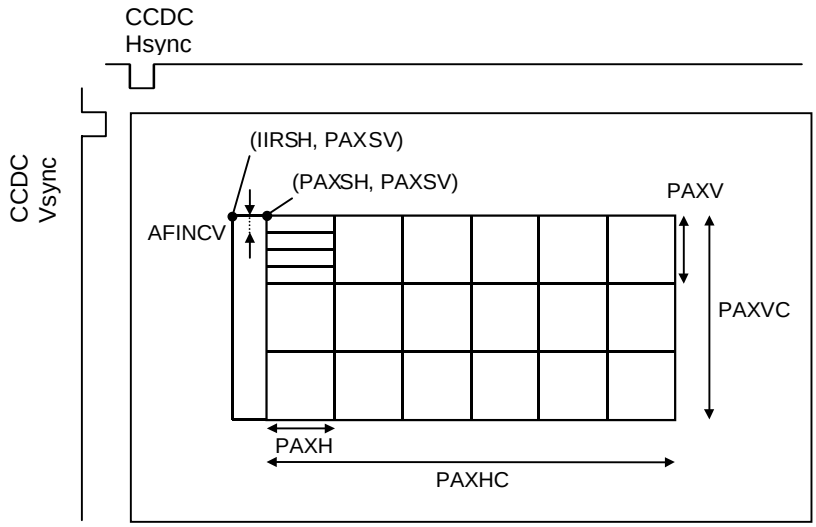


Figure 34: Paxel Configuration (green pixels only)

3.4.1 Green pixel position (GPOS)

The input signal is 8bit data, and the green pixel data is within a 2x2 window which is selected using GPOS[3:0] of AFCTRL register. Selectable green patterns are shown in the Figure 35.

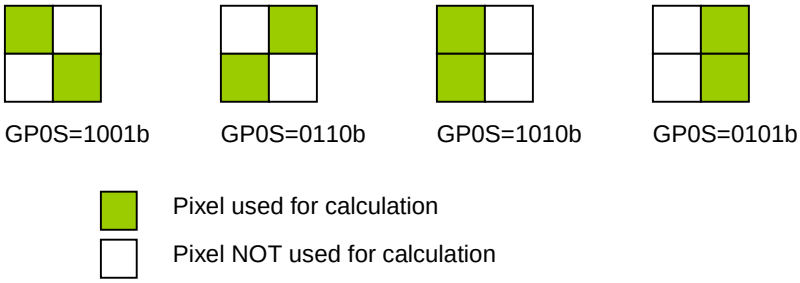


Figure 35: Sub-sampling Pattern

3.4.2 Paxel Setting

PAXH is used to set paxel width (horizontal), PAXV is used to set paxel height (vertical). Figure 36 below shows an example of setting PAXH, PAXV.

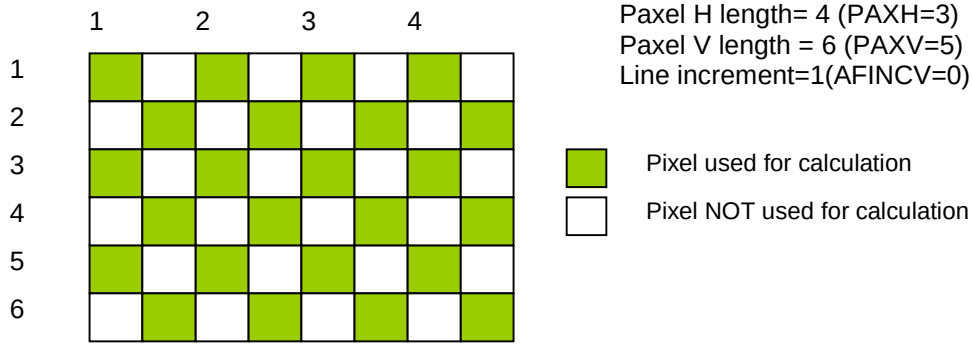


Figure 36: Paxel setting example

Note: Paxel width is number of green pixels in horizontal direction. See section 3.4.4 - Line increment also.

3.4.3 IIR Filter

There are two sets of programmable coefficient tables, AFCOEFF10 to AFCOEFF110 and AFCOEFF20 to AFCOEFF210. FV calculation is performed using both tables. Shift registers of the IIR filter are cleared to zero once in a line, at the next position of IIRSH in AFIIRSH register.

	Precision	**Range**
Filter Input	[Value of a green pixel (8bit)] – 128	-128 to 127
Coefficient	Signed 11bit (decimal 6 bit)	-16 to 15+63/64
Filter Output	Signed 12bit (decimal 4 bit)	-128 to 127+15/16

3.4.4 Line increment

Line increment within each paxel can be specified using AFINCV field in AFPAX5 register. Figure 37 shows an example of line increment within a paxel. IIR calculation is performed for only the lines selected using line increment.

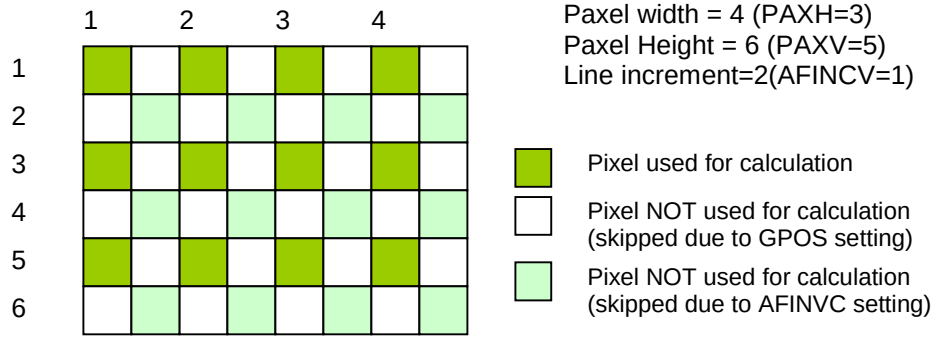


Figure 37: Line increment setting Example

3.4.5 AF Engine Output

1. Green Sum: For each paxel the green sum is output to SDRAM. This is the 32bit(23bit) in width.
2. FV sum: For each paxel the FV sum is output to SDRAM
   This is 32bit(27bit) (decimal 4bit) x 2 / Peak-FV-value Sum.

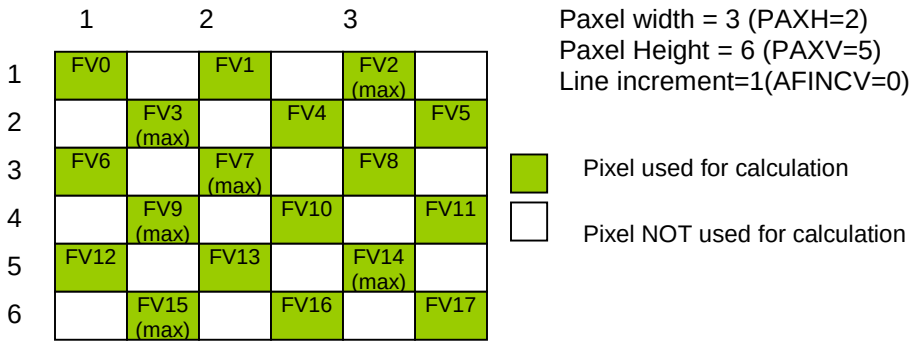


Figure 38: FV Accumalation Mode Example

Figure 38 shows an example of FV accumulation mode. Here FVn is FV value calculated by IIR filter using a coefficient table. FVn (max), is maximum FV value in a line within a paxel.

In sum mode, FV value output by AF engine for each paxel is FVout = FV0+FV1+FV2+…+FV17

In peak mode, FV value output by AF Engine for each paxel is sum of FVn max, i.e FVout = FV2+FV3+FV7+FV9+FV14+FV15

3.4.5.1 Data Transfer to SDRAM

Results of the two adjacent Paxels in a row are gathered and transferred to the SDRAM at the same time, therefore, if PAXHC is set to 2 and PAXVC is set to 1, there will be 6 sets [(PAXHC+1) x (PAXVC+1)] of data transfer within an image as shown in Figure 39. The results of the first Paxel in an image are stored to the address specified in the AFSDRA1 and AFSDRA2 registers. The address is automatically incremented until the two continuous buffers for the two successive frames become full. SDRAM buffer flag AFSDRFLG in AFSDRFLG register indicates which buffer is used to store the results.

Data transfer might fail in special cases like small PAXH number, SDRAM access waiting or ccd-sdram clock issue. DM320 report fail-condition of SDRAM-transfer to error flag register. Once error happened, AFERR bit in AFSDRFLG register gets set. It is cleared by writing '0' to it. AFERRFR0 and AFERRFR1 bits in AFSDRFLG register store the previous error status and update on each v-sync timing.

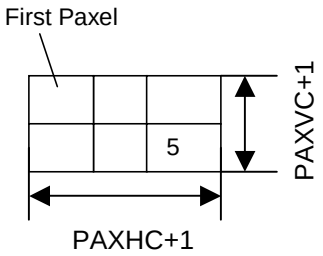


Figure 39 Exampe Paxel Configuration

In Table 16, the accumulation of green pixel values in the paxel is indicated as Green sum. The IIR filter output FV is indicated as FV sum-1, FV sum-2. These are the accumulated values using coefficient table 1 and 2 respectively. In addition, as AF result is output in sets of two paxels, when the number of horizontal paxel shown in Table 16 is odd number, dummy data is output for a paxel. The part in gray in Table 16 shows the dummy data output.

SDRAM address (byte address)	31 16	15 0	
AFSDRA	Green sum	(Paxel 0)	1st transfer start
	FV sum –1 /Peak sum -1	(Paxel 0)	
	FV sum –2 /Peak sum -2	(Paxel 0)	
	Reserved		
	Green sum	(Paxel 1)	
	FV sum –1 /Peak sum -1	(Paxel 1)	
	FV sum –2 /Peak sum -2	(Paxel 1)	
	Reserved		1st transfer end
AFSDRA + 32	Green sum	(Paxel 2)	2nd transfer start
	FV sum –1 /Peak sum -1	(Paxel 2)	
	FV sum –2 /Peak sum -2	(Paxel 2)	
	Reserved		
	Green sum	(Paxel 1)	
	FV sum –1 /Peak sum -1	(Paxel 1)	
	FV sum –2 /Peak sum -2	(Paxel 1)	
	Reserved		2nd transfer end
AFSDRA + 64	Green sum	(Paxel 3)	3rd transfer start
	FV sum –1 /Peak sum -1	(Paxel 3)	
	FV sum –2 /Peak sum -2	(Paxel 3)	
	Reserved		
	Green sum	(Paxel 4)	
	FV sum –1 /Peak sum -1	(Paxel 4)	
	FV sum –2 /Peak sum -2	(Paxel 4)	
	Reserved		3rd transfer end
AFSDRA + 96	Green sum	(Paxel 5)	4th transfer start
	FV sum –1 /Peak sum -1	(Paxel 5)	
	FV sum –2 /Peak sum -2	(Paxel 5)	
	Reserved		
	Green sum	(Paxel 4)	
	FV sum –1 /Peak sum -1	(Paxel 4)	
	FV sum –2 /Peak sum -2	(Paxel 4)	
	Reserved		4th transfer end

Table 16: AF SDRAM Output Format

3.4.5.1.1 Calculation of current SDRAM result buffer

Code below shows how to calculate the SDRAM buffer address where the AF results are stored for the previous frame.

```
Uint32 AF_getCurFrameDataAddress() {
    Uint32 dataAddr;

    dataAddr = H3A_FGET(AFSDRA1, ADRH);
    dataAddr = dataAddr << 16;
    dataAddr |= H3A_RGET(AFSDRA2);
    dataAddr *= 32;
    dataAddr += (Uint32)SDRAM_MEMORY_BASE;

    if(H3A_FGET(AFSDRFLG,AFSDRFLG)) {
       if((H3A_FGET(AFPAX2,PAXHC) + 1) & 0x1) {
           dataAddr +=
                  (H3A_FGET(AFPAX2,PAXHC) + 1 + 1) *
                  H3A_FGET(AFPAX2,PAXVC) + 1) * 16;
       } else {
           dataAddr +=
                  (H3A_FGET(AFPAX2,PAXHC) + 1) *
                  (H3A_FGET(AFPAX2,PAXVC) + 1) * 16;
       }
    }
    return dataAddr;
}
```

3.5 Auto Exposure, Auto White-Balance Engine (AEWB)

The input data to AEWB engine is the raw data output by the CCD Controller. All color component pixels (R, Gr, Gb, B) are input to the AEWB engine. The pixels in the sub-sampled 2x2 blocks are accumulated in the window as AVE1. If any of the pixels in a 2x2 block are equal to or greater than the limit value AVE2LMT, in AEWCTRL register, the block is treated as a saturated block. Only the blocks, which are not saturating are counted into CNT2. The pixels, which are clipped to AVE2LMT in the sub-sampled 2x2 blocks are accumulated in the window as AVE2, and are stored in SDRAM with AVE1.

Register	width	Description
AEWEN (H3ACTRL)	1	AE/AWB Engine enable 0:disable 1:enable
WINH (AEWWIN1)	7	Window Width (even number) ((WINH +1) x2) (2 – 256)
WINV (AEWWIN1)	6	Window Height (even number) ((WINV +1) x2) (4 – 128)
WINHC (AEWWIN2)	4	Window Count for H direction (WINHC+1) (1 – 12)
WINVC (AEWWIN2)	3	Window Count for V direction (WINVC+1) (1 – 8)
WINSH (AEWWIN3)	11	X position of the Window start point (WINSH x2) (even number)
WINSV (AEWWIN4)	11	Y position of the Window start point (WINSV x2) (even number)
AEWINCH (AEWWIN5)	4	Sampling point increments (X) in a Window (even number) ((AEWINCH+1) x2) (2-32)
AEWINCV (AEWWIN5)	4	Sampling point increments (Y) in a Window (even number) ((AEWINCV+1) x2) (2-32)
AVE2LMT (AEWCTRL)	8	AVE2 limit value
AEWSDRA (AEWSDRA1 ,	23	SDRAM destination address to store the results of AE/AWB engine. It is automatically incremented until the two continuous buffers for the two
AEWSDRFLG (AEWSDRFLG)	1	SDRAM buffer flag to indicate the buffer at which the results are stored.
AEWERRFR (AEWSDRFLG)	2	SDRAM access fail flag on previous buffer flag [0/1].
AEWERR (AEWSDRFLG)	1	SDRAM access fail flag. Clear by ARM write only.

Table 17: AEWB Configuration Registers

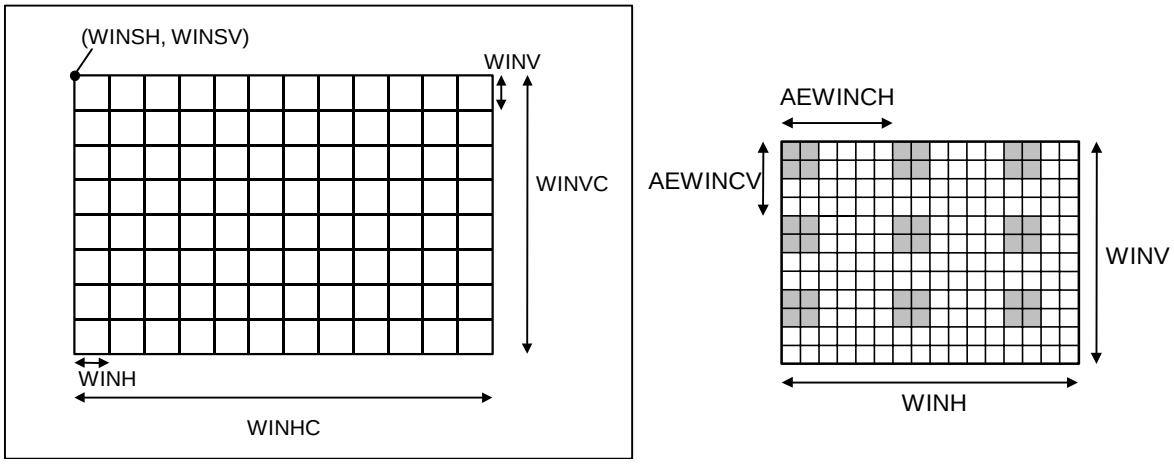


Figure 40: AEWB Window Configuration

Constraints for the configuration of AE/AWB parameters:

- The number of accumulated 2x2 blocks in a Window cannot exceed 256. WINH, WINV, AEWINCH and AEWINCV must be set accordingly.
- The number of sub-sampled pixels in a line cannot exceed 2816. WINH, WINHC and AEWINCH must be set accordingly. (Used 1408x16 line memory.)
- Windows can overlap either the first or the last line in a frame, but not both of them. WINSV, WINV and WINVC must be set accordingly.
- WINV=0 is NG. WINH=0(or small value) might be problem in data transfer to SDRAM.

3.5.1 AE/AWB Engine Output

1. AVE1[i][j] : 16bit (Array of accmulated pixels in the sub-sampled 2x2 blocks. Clipped to 65,535.)
2. AVE2[i][j] :16bit (Clipped to 65,535. Array of accumulated pixels after clipped operation to AVE2LMT in the sub-sampled 2x2 blocks)
3. CNT2[i] : 16bit(9bit) (The number of the sub-sampled 2x2 blocks which are not saturating)
4. i: window number
5. j: pixel position in 2x2 block (0:upper left, 1:upper right, 2:lower left, 3:lower right)

Table 18 shows the output of AEWB module.

3.5.2 Data transfer to SDRAM

Results of each window are transferred to the SDRAM at the same time. Therefore, if WINHC is set to 1 and WINVC is set to 1, there will be 4 sets [(WINHC+1) x (WINVC+1)] of data transfer within an image as shown in Figure 41. The results of the first Window in an image are stored to the address specified in the AEWSDRA1 and AEWSDRA2 registers. The address is automatically incremented until the two continuous buffers for the two successive frames become full. SDRAM buffer flag AEWSDRFLG in AEWSDRFLG register indicates the buffer at which the results are stored.

Data transfer might fail in special case like small WINW number, SDRAM access waiting or ccd-sdram clock issue. DM320 report fail-condition of SDRAM-transfer to error flag register. Once error happened, AEWERR bit in AEWSDRFLG register gets set. It is cleared by writing ‘0’ to it. AEWERRFR0 and AEWERRFR1 bits in AEWSDRFLG register store the previous error state and update on each v-sync timing.

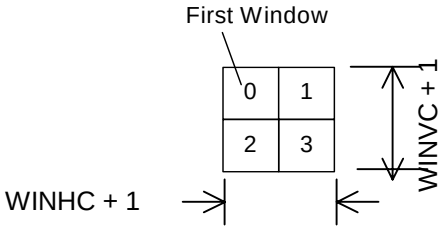


Figure 41: Example Window Configuration

NOTE: SDRAM Address is specified as offset from start of SDRAM in units of 32bytes

SDRAM address (byte address)	31 16	15 0	
AEWSDRA	AVE1[0][1]	AVE1[0][0]	1st transfer start
	AVE1[0][3]	AVE1[0][2]	
	AVE2[0][1]	AVE2[0][0]	
	AVE2[0][3]	AVE2[0][2]	
	All zero	CNT2[0]	
	All zero		
	All zero		
	All zero		1st transfer end
AEWSDRA + 32	AVE1[1][1]	AVE1[1][0]	2nd transfer start
	AVE1[1][3]	AVE1[1][2]	
	AVE2[1][1]	AVE2[1][0]	
	AVE2[1][3]	AVE2[1][2]	
	All zero	CNT2[1]	
	All zero		
	All zero		
	All zero		2nd transfer end
AEWSDRA + 64	AVE1[2][1]	AVE1[2][0]	3rd transfer start
	AVE1[2][3]	AVE1[2][2]	
	AVE2[2][1]	AVE2[2][0]	
	AVE2[2][3]	AVE2[2][2]	
	All zero	CNT2[2]	
	All zero		
	All zero		
	All zero		3rd transfer end
AEWSDRA + 96	AVE1[3][1]	AVE1[3][0]	4th transfer start
	AVE1[3][3]	AVE1[3][2]	
	AVE2[3][1]	AVE2[3][0]	
	AVE2[3][3]	AVE2[3][2]	
	All zero	CNT2[3]	
	All zero		
	All zero		
	All zero		4th transfer end

Table 18: AEWB SDRAM Data Format

3.5.3 Calculation of current SDRAM result buffer

Code below shows how to calculate the SDRAM buffer for AEWB results of the previous frame.

```
Uint32 AEWB_getCurFrameDataAddress()

{
    Uint32 dataAddr;

    dataAddr = H3A_FGET(AEWSDRA1, ADRH);
    dataAddr = dataAddr << 16;
    dataAddr |= H3A_RGET(AEWSDRA2);
    dataAddr *= 32;
    dataAddr += (Uint32)SDRAM_MEMORY_BASE;

    if(H3A_FGET(AEWSDRFLG,AEWSDRFLG)) {
         dataAddr +=
                (H3A_FGET(AEWWIN2,WINHC) + 1) *
                (H3A_FGET(AEWWIN2,WINVC) + 1) * 32;
    }
    return dataAddr;
}
```

NOTE: All registers in AF/AE/AWB Statistics Engine are latched by CCDC VD signal.

3.6 Hardware 3A register Map (H3A)

Address	Register	Description
00031B80	H3ACTRL	Hardware 3A Control Register
00031B82	AFCTRL	AF Engine Control Register
00031B84	AFPAX1	AF Engine Paxel Register #1
00031B86	AFPAX2	AF Engine Paxel Register #2
00031B88	AFPAX3	AF Engine Paxel Register #3
00031B8A	AFPAX4	AF Engine Paxel Register #4
00031B8C	AFIIRSH	AF Engine IIR Shift register
00031B8E	AFPAX5	AF Engine Paxel Register #5
00031B90	AFSDRA1	AF Engine SDRAM Address (high)
00031B92	AFSDRA2	AF Engine SDRAM Address (low)
00031B94	AFSDRFLG	AF Engine SDRAM Buffer Flag
00031B96	AFCOEFF10	AF Engine IIR Filter Table #1, Coefficient #0
00031B98	AFCOEFF11	AF Engine IIR Filter Table #1, Coefficient #1
00031B9A	AFCOEFF12	AF Engine IIR Filter Table #1, Coefficient #2
00031B9C	AFCOEFF13	AF Engine IIR Filter Table #1, Coefficient #3
00031B9E	AFCOEFF14	AF Engine IIR Filter Table #1, Coefficient #4
00031BA0	AFCOEFF15	AF Engine IIR Filter Table #1, Coefficient #5
00031BA2	AFCOEFF16	AF Engine IIR Filter Table #1, Coefficient #6
00031BA4	AFCOEFF17	AF Engine IIR Filter Table #1, Coefficient #7
00031BA6	AFCOEFF18	AF Engine IIR Filter Table #1, Coefficient #8
00031BA8	AFCOEFF19	AF Engine IIR Filter Table #1, Coefficient #9
00031BAA	AFCOEFF110	AF Engine IIR Filter Table #1, Coefficient #10
00031BAC	AFCOEFF20	AF Engine IIR Filter Table #2, Coefficient #0
00031BAE	AFCOEFF21	AF Engine IIR Filter Table #2, Coefficient #2
00031BB0	AFCOEFF22	AF Engine IIR Filter Table #2, Coefficient #2
00031BB2	AFCOEFF23	AF Engine IIR Filter Table #2, Coefficient #3
00031BB4	AFCOEFF24	AF Engine IIR Filter Table #2, Coefficient #4
00031BB6	AFCOEFF25	AF Engine IIR Filter Table #2, Coefficient #5
00031BB8	AFCOEFF26	AF Engine IIR Filter Table #2, Coefficient #6
00031BBA	AFCOEFF27	AF Engine IIR Filter Table #2, Coefficient #7
00031BBC	AFCOEFF28	AF Engine IIR Filter Table #2, Coefficient #8
00031BBE	AFCOEFF29	AF Engine IIR Filter Table #2, Coefficient #9
00031BC0	AFCOEFF210	AF Engine IIR Filter Table #2, Coefficient #20
00031BC2	AEWCTRL	AE/AWB Engine Control Register
00031BC4	AEWWIN1	AE/AWB Engine Window Register #1
00031BC6	AEWWIN2	AE/AWB Engine Window Register #2
00031BC8	AEWWIN3	AE/AWB Engine Window Register #3
00031BCA	AEWWIN4	AE/AWB Engine Window Register #4
00031BCC	AEWWIN5	AE/AWB Engine Window Register #5
00031BCE	AEWSDRA1	AE/AWB Engine SDRAM Address (high)
00031BD0	AEWSDRA2	AE/AWB Engine SDRAM Address (low)
00031BD2	AEWSDRFLG	AE/AWB Engine SDRAM Buffer Flag

3.7 Hardware 3A Registers

3.7.1 H3ACTRL

Hardware 3A Control Register

H3ACTRL 0003:0B80 offset: 0x00 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AEWEN	RSV	RSV	RSV	AFEN
R/W	-	-	-	-	-	-	-	-	-	-	-	R/W	-	-	-	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	0

Bit	Name	Reset Value	R/W	Function
15:5	RSV			Reserved
4	AEWEN	0	R/W	AE/AWB Engine enable. » 0: Disable « » 1: Enable «
3:1	RSV			Reserved
0	AFEN	0	R/W	AF Engine enable. » 0: Disable « » 1: Enable «

3.7.2 AFCTRL

AF Engine Control Register

AFCTRL 0003:0B82 offset: 0x02 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	FVMODE	GPOSUL	GPOSUR	GPOSLL	GPOSLR
R/W	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:5	RSV			Reserved
4	FVMODE	0	R/W	[AF Engine] Focus Value(FV) accumulation mode. » 0: Sum mode « » 1: Peak mode «
3	GPOSUL	0	R/W	[AF Engine] Green pixel extraction. upper left in 2x2 block (even pixel, even line). » 0: Other than green « » 1: Green «
2	GPOSUR	0	R/W	[AF Engine] Green pixel extraction. upper right in 2x2 block (odd pixel, even line). » 0: Other than green « » 1: Green «
1	GPOSLL	0	R/W	[AF Engine] Green pixel extraction. lower left in 2x2 block (even pixel, odd line). » 0: Other than green « » 1: Green «
0	GPOSLR	0	R/W	[AF Engine] Green pixel extraction. lower right in 2x2 block (odd pixel, odd line). » 0: Other than green « » 1: Green «

3.7.3 AFPAX1

AF Engine Paxel Register #1

AFPAX1 0003:0B84 offset: 0x04 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	PAXV[6]	PAXV[5]	PAXV[4]	PAXV[3]	PAXV[2]	PAXV[1]	PAXV[0]	PAXH[7]	PAXH[6]	PAXH[5]	PAXH[4]	PAXH[3]	PAXH[2]	PAXH[1]	PAXH[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	PAXV	0	R/W	[AF Engine] Paxel Height (number of green lines). Paxel Height is (PAXV +1) and ranges: 2-128. A value greater than 0 must be set to PAXV.
7:0	PAXH	0	R/W	[AF Engine] Paxel Width (number of green pixels). Paxel Width is (PAXH +1) and ranges: 1-256. Setting a small value to PAXH might collapse the data transfer to SDRAM. SDRAM access time can not be longer than the time it takes for the Paxel Width (PAXH+1). SDRAM access time varies depending on CCD and SDRAM clock frequency settings, and also the status of the other peripherals' access to SDRAM.

3.7.4 AFPAX2

AF Engine Paxel Register #2

AFPAX2 0003:0B86 offset: 0x06 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	PAXVC[2]	PAXVC[1]	PAXVC[0]	RSV	RSV	RSV	RSV	PAXHC[3]	PAXHC[2]	PAXHC[1]	PAXHC[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	-	-	-	-	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	-	-	-	-	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:8	PAXVC	0	R/W	[AF Engine] Paxel Count for V direction. Paxel Count is (PAXVC +1) and ranges: 1-8.
7:4	RSV			Reserved
3:0	PAXHC	0	R/W	[AF Engine] Paxel Count for H direction. Paxel Count is (PAXHC +1) and ranges: 1-12. Setting a value greater than 11 to PAXHC is not allowed.

3.7.5 AFPAX3

AF Engine Paxel Register #3

AFPAX3 0003:0B88 offset: 0x08 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	PAXSH[11]	PAXSH[10]	PAXSH[9]	PAXSH[8]	PAXSH[7]	PAXSH[6]	PAXSH[5]	PAXSH[4]	PAXSH[3]	PAXSH[2]	PAXSH[1]	PAXSH[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	PAXSH	0	R/W	[AF Engine] Paxel start position (H direction, green pixels). Range: 1-4,095. PAXSH must be equal to or greater than (IIRSH + 1).

3.7.6 AFPAX4

AF Engine Paxel Register #4

AFPAX4 0003:0B8A offset: 0x0A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	PAXSV[11]	PAXSV[10]	PAXSV[9]	PAXSV[8]	PAXSV[7]	PAXSV[6]	PAXSV[5]	PAXSV[4]	PAXSV[3]	PAXSV[2]	PAXSV[1]	PAXSV[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	PAXSV	0	R/W	[AF Engine] Paxel start position (V direction, green lines). Range: 0-4,095.

3.7.7 AFIIRSH

AF Engine IIR Shift register

AFIIRSH 0003:0B8C offset: 0x0C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	IIRSH[11]	IIRSH[10]	IIRSH[9]	IIRSH[8]	IIRSH[7]	IIRSH[6]	IIRSH[5]	IIRSH[4]	IIRSH[3]	IIRSH[2]	IIRSH[1]	IIRSH[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	IIRSH	0	R/W	[AF Engine] IIR filter start position (H direction, green pixels). Range: 0-4,095. Shift registers of the IIR filter are cleared to zero at the next position of IIRSH.

3.7.8 AFPAX5

AF Engine Paxel Register #5

AFPAX5 0003:0B8E offset: 0x0E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	AFINCV[3]	AFINCV[2]	AFINCV[1]	AFINCV[0]	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
R/W	-	-	-	-	R/W	R/W	R/W	R/W	-	-	-	-	-	-	-	-
Default	-	-	-	-	0	0	0	0	-	-	-	-	-	-	-	-

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:8	AFINCV	0	R/W	[AF Engine] Line increments in a Paxel (number of green lines). Increments are (AFINCV +1) and ranges: 1-16.
7:0	RSV			Reserved

3.7.9 AFSDRA1

AF Engine SDRAM Address (high)

AFSDRA1 0003:0B90 offset: 0x10 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADRH[6]	ADRH[5]	ADRH[4]	ADRH[3]	ADRH[2]	ADRH[1]	ADRH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	ADRH	0	R/W	[AF Engine] Upper 7 bits of SDRAM destination address to store the results of AF engine. There are two continuous buffers, and the results of the two successive frames are stored to the different buffers. Buffer size depends on PAXHC and PAXVC. AFSDRA is the start address of the first buffer, and the address is automatically incremented until data transfer for the two frame ends (address is 32 Byte unit) specified as offset from start of SDRAM.

3.7.10 AFSDRA2

AF Engine SDRAM Address (low)

AFSDRA2 0003:0B92 offset: 0x12 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADRL[15]	ADRL[14]	ADRL[13]	ADRL[12]	ADRL[11]	ADRL[10]	ADRL[9]	ADRL[8]	ADRL[7]	ADRL[6]	ADRL[5]	ADRL[4]	ADRL[3]	ADRL[2]	ADRL[1]	ADRL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	ADRL	0	R/W	[AF Engine] Lower 16 bits of SDRAM destination address to store the results of AF engine. There are two continuous buffers, and the results of the two successive frames are stored to the different buffers. Buffer size depends on PAXHC and PAXVC. AFSDRA is the start address of the first buffer, and the address is automatically incremented until data transfer for the two frame ends (address is 32 Byte unit) specified as offset from start of SDRAM.

3.7.11 AFSDRFLG

AF Engine SDRAM Buffer Flag

AFSDRFLG 0003:0B94 offset: 0x14 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AFERR	AFERRFR1	AFERRFR0	RSV	RSV	RSV	AFSDRFLG
R/W	-	-	-	-	-	-	-	-	-	R/W	R	R	-	-	-	R
Default	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6	AFERR	0	R/W	SDRAM access fail flag, Clear by ARM write
5	AFERRFR1	0	R	SDRAM access fail on previous buffer flag 1
4	AFERRFR0	0	R	SDRAM access fail on previous buffer flag 0
3:1	RSV			Reserved
0	AFSDRFLG	0	R	SDRAM buffer flag to indicate the buffer at which the results of the last frame is stored. » 0: Results stored at first buffer starting from AFSDRA « » 1: Results are stored at the second buffer «

3.7.12 AFCOEFF10

AF Engine IIR Filter Table #1, Coefficient #0

AFCOEFF10 0003:0B96 offset: 0x16 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF10[10]	COEFF10[9]	COEFF10[8]	COEFF10[7]	COEFF10[6]	COEFF10[5]	COEFF10[4]	COEFF10[3]	COEFF10[2]	COEFF10[1]	COEFF10[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF10	0	R/W	[AF Engine] IIR filter Coefficient #0 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.13 AFCOEFF11

AF Engine IIR Filter Table #1, Coefficient #1

AFCOEFF11 0003:0B98 offset: 0x18 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF11[10]	COEFF11[9]	COEFF11[8]	COEFF11[7]	COEFF11[6]	COEFF11[5]	COEFF11[4]	COEFF11[3]	COEFF11[2]	COEFF11[1]	COEFF11[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF11	0	R/W	[AF Engine] IIR filter Coefficient #1 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.14 AFCOEFF12

AF Engine IIR Filter Table #1, Coefficient #2

AFCOEFF12 0003:0B9A offset: 0x1A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF12[10]	COEFF12[9]	COEFF12[8]	COEFF12[7]	COEFF12[6]	COEFF12[5]	COEFF12[4]	COEFF12[3]	COEFF12[2]	COEFF12[1]	COEFF12[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF12	0	R/W	[AF Engine] IIR filter Coefficient #2 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.15 AFCOEFF13

AF Engine IIR Filter Table #1, Coefficient #3

AFCOEFF13 0003:0B9C offset: 0x1C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF13[10]	COEFF13[9]	COEFF13[8]	COEFF13[7]	COEFF13[6]	COEFF13[5]	COEFF13[4]	COEFF13[3]	COEFF13[2]	COEFF13[1]	COEFF13[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF13	0	R/W	[AF Engine] IIR filter Coefficient #3 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.16 AFCOEFF14

AF Engine IIR Filter Table #1, Coefficient #4

AFCOEFF14 0003:0B9E offset: 0x1E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF14[1	COEFF14[9	COEFF14[8	COEFF14[7	COEFF14[6	COEFF14[5]	COEFF14[4]	COEFF14[3	COEFF14[2	COEFF14[1	COEFF14[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF14	0	R/W	[AF Engine] IIR filter Coefficient #4 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.17 AFCOEFF15

AF Engine IIR Filter Table #1, Coefficient #5

AFCOEFF15 0003:0BA0 offset: 0x20 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF15[1	COEFF15[9	COEFF15[8	COEFF15[7	COEFF15[6	COEFF15[5]	COEFF15[4]	COEFF15[3	COEFF15[2	COEFF15[1	COEFF15[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF15	0	R/W	[AF Engine] IIR filter Coefficient #5 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.18 AFCOEFF16

AF Engine IIR Filter Table #1, Coefficient #6

AFCOEFF16 0003:0BA2 offset: 0x22 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF16[1	COEFF16[9	COEFF16[8	COEFF16[7	COEFF16[6	COEFF16[5]	COEFF16[4]	COEFF16[3	COEFF16[2	COEFF16[1	COEFF16[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF16	0	R/W	[AF Engine] IIR filter Coefficient #6 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.19 AFCOEFF17

AF Engine IIR Filter Table #1, Coefficient #7

AFCOEFF17 0003:0BA4 offset: 0x24 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF17[10	COEFF17[9	COEFF17[8	COEFF17[7	COEFF17[6	COEFF17[5]	COEFF17[4]	COEFF17[3	COEFF17[2	COEFF17[1	COEFF17[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF17	0	R/W	[AF Engine] IIR filter Coefficient #7 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.20 AFCOEFF18

AF Engine IIR Filter Table #1, Coefficient #8

AFCOEFF18 0003:0BA6 offset: 0x26 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF18[10	COEFF18[9	COEFF18[8	COEFF18[7	COEFF18[6	COEFF18[5]	COEFF18[4]	COEFF18[3	COEFF18[2	COEFF18[1	COEFF18[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF18	0	R/W	[AF Engine] IIR filter Coefficient #8 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.21 AFCOEFF19

AF Engine IIR Filter Table #1, Coefficient #9

AFCOEFF19 0003:0BA8 offset: 0x28 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF19[10	COEFF19[9	COEFF19[8	COEFF19[7	COEFF19[6	COEFF19[5]	COEFF19[4]	COEFF19[3	COEFF19[2	COEFF19[1	COEFF19[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF19	0	R/W	[AF Engine] IIR filter Coefficient #9 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.22 AFCOEFF110

AF Engine IIR Filter Table #1, Coefficient #10

AFCOEFF110 0003:0BAA offset: 0x2A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF110[1	COEFF110[9	COEFF110[8	COEFF110[7	COEFF110[6	COEFF110[5]	COEFF110[4]	COEFF110[3	COEFF110[2	COEFF110[1	COEFF110[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF110	0	R/W	[AF Engine] IIR filter Coefficient #10 <Table1>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.23 AFCOEFF20

AF Engine IIR Filter Table #2, Coefficient #0

AFCOEFF20 0003:0BAC offset: 0x2C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF20[1	COEFF20[9	COEFF20[8	COEFF20[7	COEFF20[6	COEFF20[5]	COEFF20[4]	COEFF20[3	COEFF20[2	COEFF20[1	COEFF20[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF20	0	R/W	[AF Engine] IIR filter Coefficient #0 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.24 AFCOEFF21

AF Engine IIR Filter Table #2, Coefficient #1

AFCOEFF21 0003:0BAE offset: 0x2E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF21[1	COEFF21[9	COEFF21[8	COEFF21[7	COEFF21[6	COEFF21[5]	COEFF21[4]	COEFF21[3	COEFF21[2	COEFF21[1	COEFF21[0
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF21	0	R/W	[AF Engine] IIR filter Coefficient #1 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.25 AFCOEFF22

AF Engine IIR Filter Table #2, Coefficient #2

AFCOEFF22 0003:0BB0 offset: 0x30 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF22[10]	COEFF22[9]	COEFF22[8]	COEFF22[7]	COEFF22[6]	COEFF22[5]	COEFF22[4]	COEFF22[3]	COEFF22[2]	COEFF22[1]	COEFF22[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF22	0	R/W	[AF Engine] IIR filter Coefficient #2 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.26 AFCOEFF23

AF Engine IIR Filter Table #2, Coefficient #3

AFCOEFF23 0003:0BB2 offset: 0x32 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF23[10]	COEFF23[9]	COEFF23[8]	COEFF23[7]	COEFF23[6]	COEFF23[5]	COEFF23[4]	COEFF23[3]	COEFF23[2]	COEFF23[1]	COEFF23[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF23	0	R/W	[AF Engine] IIR filter Coefficient #3 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.27 AFCOEFF24

AF Engine IIR Filter Table #2, Coefficient #4

AFCOEFF24 0003:0BB4 offset: 0x34 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF24[10]	COEFF24[9]	COEFF24[8]	COEFF24[7]	COEFF24[6]	COEFF24[5]	COEFF24[4]	COEFF24[3]	COEFF24[2]	COEFF24[1]	COEFF24[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF24	0	R/W	[AF Engine] IIR filter Coefficient #4 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.28 AFCOEFF25

AF Engine IIR Filter Table #2, Coefficient #5

AFCOEFF25 0003:0BB6 offset: 0x36 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF25[1	COEFF25[9	COEFF25[8	COEFF25[7	COEFF25[6	COEFF25[5]	COEFF25[4]	COEFF25[3	COEFF25[2	COEFF25[1	COEFF25[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF25	0	R/W	[AF Engine] IIR filter Coefficient #5 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.29 AFCOEFF26

AF Engine IIR Filter Table #2, Coefficient #6

AFCOEFF26 0003:0BB8 offset: 0x38 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF26[1	COEFF26[9	COEFF26[8	COEFF26[7	COEFF26[6	COEFF26[5]	COEFF26[4]	COEFF26[3	COEFF26[2	COEFF26[1	COEFF26[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF26	0	R/W	[AF Engine] IIR filter Coefficient #6 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.30 AFCOEFF27

AF Engine IIR Filter Table #2, Coefficient #7

AFCOEFF27 0003:0BBA offset: 0x3A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF27[1	COEFF27[9	COEFF27[8	COEFF27[7	COEFF27[6	COEFF27[5]	COEFF27[4]	COEFF27[3	COEFF27[2	COEFF27[1	COEFF27[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF27	0	R/W	[AF Engine] IIR filter Coefficient #7 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.31 AFCOEFF28

AF Engine IIR Filter Table #2, Coefficient #8

AFCOEFF28 0003:0BBC offset: 0x3C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF28[10]	COEFF28[9]	COEFF28[8]	COEFF28[7]	COEFF28[6]	COEFF28[5]	COEFF28[4]	COEFF28[3]	COEFF28[2]	COEFF28[1]	COEFF28[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF28	0	R/W	[AF Engine] IIR filter Coefficient #8 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.32 AFCOEFF29

AF Engine IIR Filter Table #2, Coefficient #9

AFCOEFF29 0003:0BBE offset: 0x3E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF29[10]	COEFF29[9]	COEFF29[8]	COEFF29[7]	COEFF29[6]	COEFF29[5]	COEFF29[4]	COEFF29[3]	COEFF29[2]	COEFF29[1]	COEFF29[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF29	0	R/W	[AF Engine] IIR filter Coefficient #9 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.33 AFCOEFF210

AF Engine IIR Filter Table #2, Coefficient #10

AFCOEFF210 0003:0BC0 offset: 0x40 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	COEFF210[10]	COEFF210[9]	COEFF210[8]	COEFF210[7]	COEFF210[6]	COEFF210[5]	COEFF210[4]	COEFF210[3]	COEFF210[2]	COEFF210[1]	COEFF210[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	COEFF210	0	R/W	[AF Engine] IIR filter Coefficient #10 <Table2>. Decimal 6 bit: -16≦coeff≦15+63/64

3.7.34 AEWCTRL

AE/AWB Engine Control Register

AEWCTRL 0003:0BC2 offset: 0x42 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AVE2LMT[7]	AVE2LMT[6]	AVE2LMT[5]	AVE2LMT[4]	AVE2LMT[3]	AVE2LMT[2]	AVE2LMT[1]	AVE2LMT[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	AVE2LMT	0	R/W	[AE/AWB Engine] Saturation limit. Note: If any of the pixels in a 2x2 block are equal to or greater than AVE2LMT, the block is treated as a saturated data, and not counted into CNT2. If a sub-sampled 2x2 block is saturating, the pixels equal to or greater than AVE2LMT are clipped to AVE2LMT, and accumulated to AVE2.

3.7.35 AEWWIN1

AE/AWB Engine Window Register #1

AEWWIN1 0003:0BC4 offset: 0x44 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	WINV[5]	WINV[4]	WINV[3]	WINV[2]	WINV[1]	WINV[0]	RSV	WINH[6]	WINH[5]	WINH[4]	WINH[3]	WINH[2]	WINH[1]	WINH[0]
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	RSV			Reserved
13:8	WINV	0	R/W	[AE/AWB Engine] Window Height (even number). Window Height is ((WINV +1) x2) ranges: 4-128
7	RSV			Reserved
6:0	WINH	0	R/W	[AE/AWB Engine] Window Width (even number). Window Width is ((WINH +1) x2) and ranges: 2-256

3.7.36 AEWWIN2

AE/AWB Engine Window Register #2

AEWWIN2 0003:0BC6 offset: 0x46 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	WINVC[2]	WINVC[1]	WINVC[0]	RSV	RSV	RSV	RSV	WINHC[3]	WINHC[2]	WINHC[1]	WINHC[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	-	-	-	-	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	-	-	-	-	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:8	WINVC	0	R/W	[AE/AWB Engine] Window Count for V direction. Window Count is (WINVC +1) and ranges: 1-8.
7:4	RSV			Reserved
3:0	WINHC	0	R/W	[AE/AWB Engine] Window Count for H direction. Window Count is (WINHC +1) and ranges: 1-12. Setting a value greater than 11 to WINHC is not allowed.

3.7.37 AEWWIN3

AE/AWB Engine Window Register #3

AEWWIN3 0003:0BC8 offset: 0x48 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	WINSH[10]	WINSH[9]	WINSH[8]	WINSH[7]	WINSH[6]	WINSH[5]	WINSH[4]	WINSH[3]	WINSH[2]	WINSH[1]	WINSH[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	WINSH	0	R/W	[AE/AWB Engine] Window start position (H direction, even number). Window start position is (WINSH x2) and ranges: 0-4,094

3.7.38 AEWWIN4

AE/AWB Engine Window Register #4

AEWWIN4 0003:0BCA offset: 0x4A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	WINSV[10]	WINSV[9]	WINSV[8]	WINSV[7]	WINSV[6]	WINSV[5]	WINSV[4]	WINSV[3]	WINSV[2]	WINSV[1]	WINSV[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	WINSV	0	R/W	[AE/AWB Engine] Window start position (V direction, even number). Window start position is (WINSV x2) and ranges: 0-4,094

3.7.39 AEWWIN5

AE/AWB Engine Window Register #5

AEWWIN5 0003:0BCC offset: 0x4C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	AEWINCV[3	AEWINCV[2	AEWINCV[1	AEWINCV[0	RSV	RSV	RSV	RSV	AEWINCH[3	AEWINCH[2	AEWINCH[1	AEWINCH[0
R/W	-	-	-	-	R/W	R/W	R/W	R/W	-	-	-	-	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	-	-	-	-	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:8	AEWINCV	0	R/W	[AE/AWB Engine] Sampling point increments in a Window (V direction, even number). Increments are ((AEWINCV +1) x2) and ranges: 2-32
7:4	RSV			Reserved
3:0	AEWINCH	0	R/W	[AE/AWB Engine] Sampling point increments in a Window (H direction, even number). Increments are ((AEWINCH +1) x2) and ranges: 2-32

3.7.40 AEWSDRA1

AE/AWB Engine SDRAM Address (high)

AEWSDRA1 0003:0BCE offset: 0x4E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADRH[6]	ADRH[5]	ADRH[4]	ADRH[3]	ADRH[2]	ADRH[1]	ADRH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	ADRH	0	R/W	[AE/AWB Engine] Upper 7 bits of SDRAM destination address to store the results of AE/AWB Engine. There are two continuous buffers, and the results of the two successive frames are stored to the different buffers. Buffer size depends on WINHC and WINVC. AEWSDRA is the start address of the first buffer, and the address is automatically incremented until data transfer for the two frame ends (address is 32 Byte unit) specified as offset from start of SDRAM.

3.7.41 AEWSDRA2

AE/AWB Engine SDRAM Address (low)

AEWSDRA2 0003:0BD0 offset: 0x50 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADRL[15]	ADRL[14]	ADRL[13]	ADRL[12]	ADRL[11]	ADRL[10]	ADRL[9]	ADRL[8]	ADRL[7]	ADRL[6]	ADRL[5]	ADRL[4]	ADRL[3]	ADRL[2]	ADRL[1]	ADRL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	ADRL	0	R/W	[AE/AWB Engine] Lower 16 bits of SDRAM destination address to store the results of AE/AWB Engine. There are two continuous buffers, and the results of the two successive frames are stored to the different buffers. Buffer size depends on WINHC and WINVC. AEWSDRA is the start address of the first buffer, and the address is automatically incremented until data transfer for the two frame ends (address is 32 Byte unit) specified as offset from start of SDRAM.

3.7.42 AEWSDRFLG

AE/AWB Engine SDRAM Buffer Flag

AEWSDRFLG 0003:0BD2 offset: 0x52 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AEWERR	AEWERRFR1	AEWERRFR0	RSV	RSV	RSV	EWSDRFL(
R/W	-	-	-	-	-	-	-	-	-	R/W	R	R	-	-	-	R
Default	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6	AEWERR	0	R/W	SDRAM access fail flag, Clear by ARM write
5	AEWERRFR1	0	R	SDRAM access fail flag om previous buffer flag 1
4	AEWERRFR0	0	R	SDRAM access fail flag om previous buffer flag 0
3:1	RSV			Reserved
0	AEWSDRFLG	0	R	[AE/AWB Engine] SDRAM buffer flag to indicate the buffer at which the results of the last frame are stored. » 0: Results stored at first buffer starting AEWSDRA « » 1: Results are stored at the second buffer «

4 OSD - On-Screen Display

4.1 Introduction

The OSD graphic accelerator is responsible for managing OSD data from different OSD windows and blending it with the video. It reads OSD data from SDRAM, and outputs it to the on-chip Video Encoder. After being configured and activated by the ARM, the OSD reads OSD data and mixes it with the video output. ARM is responsible for configuration and control of OSD operations and writing of the OSD data to the SDRAM.

4.2 Features

- Two Video Windows
- One bitmap Window + Attribute window, or two bitmap windows
- One of the OSD window can be configured as RGB16 window
- One rectangular Cursor Window
- Color Palette ROM/RAM selection
- Programmable Color Palette
- All Windows can be blended and displayed
- Video Window Zoom (x2,x4,H/V)
- Video Window Field/Frame selection
- Bitmap Window Zoom (x2,x4,H/V)
- Bitmap Window Field/Frame selection
- Resize of VGA to NTSC/PAL
- Back Ground color selection
- Selectable bitmap width of 1,2,4,8-bit
- Blending of Video and OSD data (8-step)
- 16-LUT registers for OSD Window
- Cursor Display with Width and color selectable
- Ping Pong Buffer Control with H/W Signal
- Polarity Selection of Field Signal
- Configurable CbCr order

4.3 OSD Block Diagram

The *Figure 42* shows the OSD block diagram.

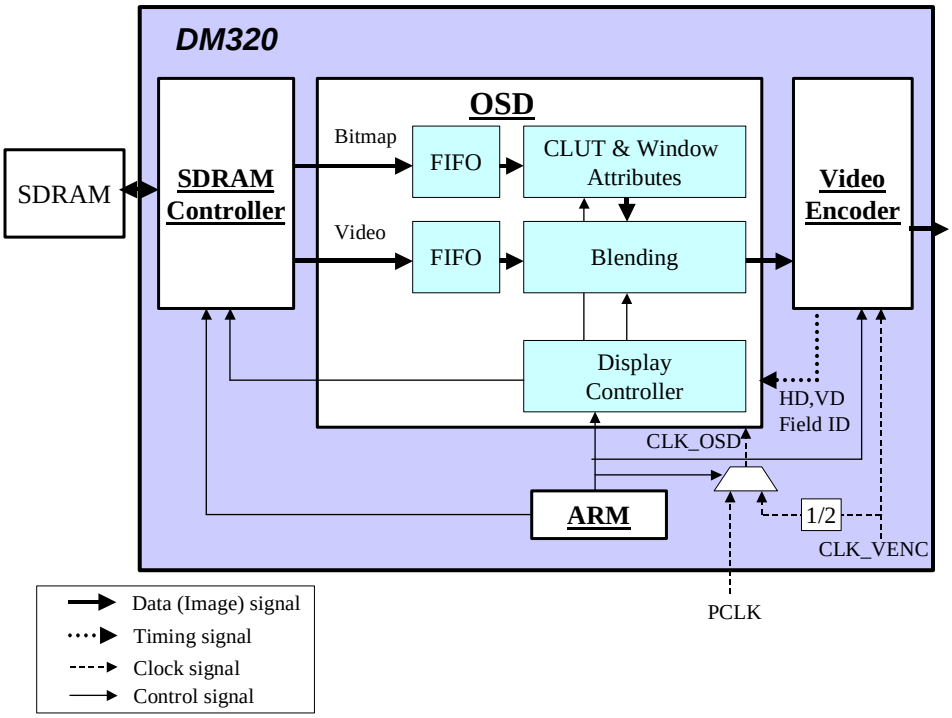


Figure 42: OSD Block Diagram

4.4 Bitmap and Video Windows

OSD supports the following windows:

- OSD Video Window 0 (Main Video Window)– displays YCbCr 4:2:2 video data
- OSD Video Window 1 – displays YCbCr 4:2:2 video data
- OSD Bitmap Window 0 – displays 1,2,4,8-bit bitmap data using color lookup table or RGB16 data
- OSD Bitmap Window 1 – displays 1,2,4,8-bit bitmap data using color lookup table / RGB16 data or OSD Attribute Window – for pixel level blending of OSD Bitmap Window 0 and video window 0,1
- Rectangular Hardware cursor

Register	Description
VIDWINMD	Controls the display, zoom and on/off control of Video windows
OSDWIN0MD	Controls the display, zoom blending, and on/off control of OSD window 0
OSDWIN1MD	Controls the display, zoom blending, and on/off control of OSD window 1
OSDATRMD	Controls the blinking, display, zoom, on/off control of Attribute window
RECTCUR	Controls the size and on/off control of rectangular cursor window

If overlapping occurs between different windows, the color of each displayed pixel corresponds to the color of the window with the highest priority. The priority order is fixed. When OSD bitmap window 1 is configured to be in attribute mode, its priority does not change. Figure 43 illustrates the priority of different windows. Video Window 0 and 1 should not overlap with the OSD window if the window is set to RGB 16 mode.

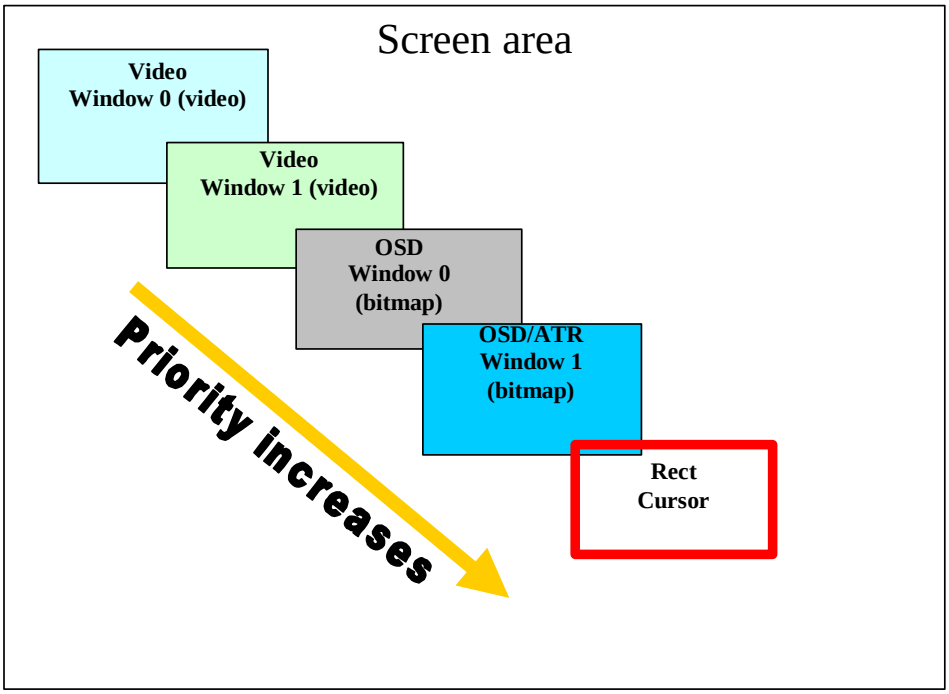


Figure 43: OSD Window Priority

4.5 OSD Window Data Storage Format

In the bitmap window, each pixel can be 1, 2, 4, or 8 bits wide. In the YCbCr 4:2:2 window, each Y, Cb, Cr component takes 8-bit, and the components are arranged according to 4:2:2 interleaved format (Cb-Y-Cr-Y-…). In case RGB graphics data needs to be displayed using OSD, the application should perform software conversion to Y,Cr,Cb before storing it. The OSD data is always packed into 32-bit words and left justified. Starting from the upper left corner of

the OSD window, all data will be packed into adjacent 32-bit words. Figure 44 shows data format of video, bitmap data in SDRAM.

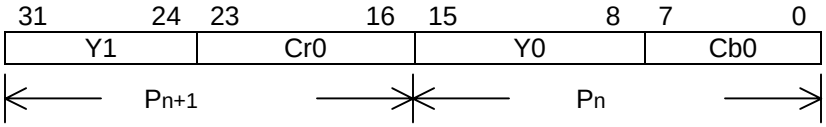
(a) Left top

Pixel arrangement in the display

P0	P1	P2	P3	P4	P5	P6	P7…

(b) Video Data (Video Window 0, 1)

16-bit per pixel

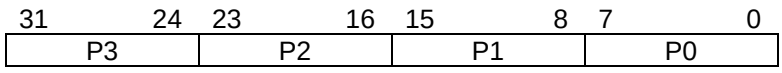


SDRAM format

Address	31 16	0
N	P1	P0
N+1	P3	P2
N+2	P5	P4
…	…	…

(c) Bitmap Data (OSD Bitmap Window 0, 1)

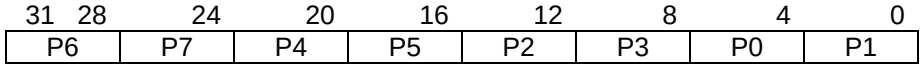
8-bit per pixel



SDRAM format

Address	31 24	16	8	0
N	P3	P2	P1	P0
N+1	P7	P6	P5	P4
N+2	P11	P10	P9	P8
…	…	…	…	…

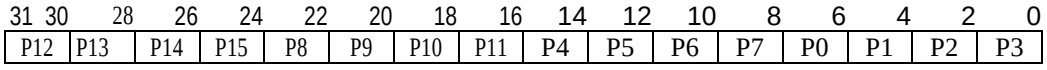
4-bit per pixel



SDRAM format

Address	31 28	24	20	16	12	8	4	0
N	P6	P7	P4	P5	P2	P3	P0	P1
N+1	P14	P15	P12	P13	P10	P11	P8	P9
N+2	P22	P23	P20	P21	P18	P19	P16	P17
N+3								

2-bit per pixel



SDRAM format

Address	31 30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
N	P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3
N+1	P28	P29	P30	P31	P24	P25	P26	P27	P20	P21	P22	P23	P16	P17	P18	P19
N+2	P44	P45	P46	P47	P40	P41	P42	P43	P36	P37	P38	P39	P32	P33	P34	P35
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

1-bit per pixel

31 0

P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7

SDRAM format

Address	31															0
N	P24	P25	P26~P3											P4	P5	P6	P7
N+1	P56	P57	P58~P35											P36	P37	P38	P39
N+2	P88	P89	P90~P67											P68	P69	P70	P71
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

(d) RGB 16bit data for OSD window

SDRAM Format

Address	31	26	20	15	10	4
N	P1 (Red)	P1 (Green)	P1 (Blue)	P0 (Red)	P0 (Green)	P0 (Blue)
N+1	P3 (Red)	P3 (Green)	P3 (Blue)	P2 (Red)	P2 (Green)	P2 (Blue)
N+2	P5 (Red)	P5 (Green)	P5 (Blue)	P4 (Red)	P4 (Green)	P4 (Blue)
…	…	…	…	…	…	…

Figure 44 OSD SDRAM Data Format

4.6 OSD Configuration and Control

Many of the OSD registers contain bits that are latched by the VD signal, which is the vertical sync pulse generated by the DM320's Video Encoder module. Data written to a latched bit does not take affect until the VD pulse is received. This allows registers that control the OSD, such as the SDRAM data address, display window size, display zoom configuration, etc. to be changed in between successive VD pulses without corrupting the current display. In the OSD register descriptions, bit fields marked with (*) are latched by the VD signal.

4.6.1 SDRAM location and offset

The location of data stored in SDRAM is defined by several memory-mapped registers (see *Table 19*). The SDRAM addresses are specified in units of 32 bytes, since data is transferred from SDRAM to the OSD hardware in bursts of

32 bytes. SDRAM address is specified as offset from start of SDRAM region. SDRAM address must be 32byte aligned.

For example, let the video window 0 video data be located at absolute SDRAM address 0x97AB00. The address register would be set as shown in the code below.

```
Uint32 window_addr;

window_addr = (0x97AB00 – 0x900000)/32;

OSD_FSET( VIDWINADH, V0AH, window_addr >> 16);
OSD_RSET( VIDWIN0ADL, window_addr & 0xFFFF);
```

SDRAM address location register	Window
VIDWINADH VIDWIN0ADL	Video Window 0 low and high address
VIDWINADH VIDWIN1ADL	Video Window 1 low and high address
OSDWINADH OSDWIN0ADL	OSD Bitmap Window 0 low and high address
OSDWINADH OSDWIN1ADL	OSD Bitmap Window 1 / Attribute Window low and high address

Table 19: SDRAM address location registers

The offset registers allow a cropped segment of an image to be easily displayed. An offset register specifies the distance, in SDRAM, from the start of a displayed line to the start of the next displayed line. The offset is in units of 32 bytes. Thus width of data stored in SDRAM must be multiple of 32bytes. In case, the width of data in SDRAM is not multiple of 32bytes, then padding must be done to make it multiple of 32bytes.

Table 20 shows the registers for controlling the SDRAM offset for video and bitmap windows.

For example, for OSD bitmap window 0, with 4-bit pixel width, If the width of the bitmap is “size” pixels. Since for 4-bit bitmap, two pixels is one byte. Hence width of data stored in SDRAM would be “size / 2” bytes and offset register would be set as shown in the code below.

```
Uint32 addr = size / 2;

OSD_RSET(OSDWIN0OFST, addr/32 );
```

SDRAM offset register	Window
VIDWIN0OFST	Video Window 0 SDRAM offset register
VIDWIN1OFST	Video Window 1 SDRAM offset register
OSDWIN0OFST	OSD Bitmap Window 0 SDRAM offset register
OSDWIN1OFST	OSD Bitmap Window 1 / Attribute Window SDRAM offset register

Table 20: SDRAM offset registers

Note: The size restriction is only applicable for bitmap windows.

4.6.2 Windows positioning

The windows use a common reference pixel (base pixel). The position of this pixel is determined from the beginning of the Video Encoder HD and the beginning of the Video Encoder VD signal.

For each window (video or bitmap) and for the cursor, the location of the upper left corner can be specified. The display size of the window needs to be specified as well. The relationship of the display positions of each window is shown in Figure 45.

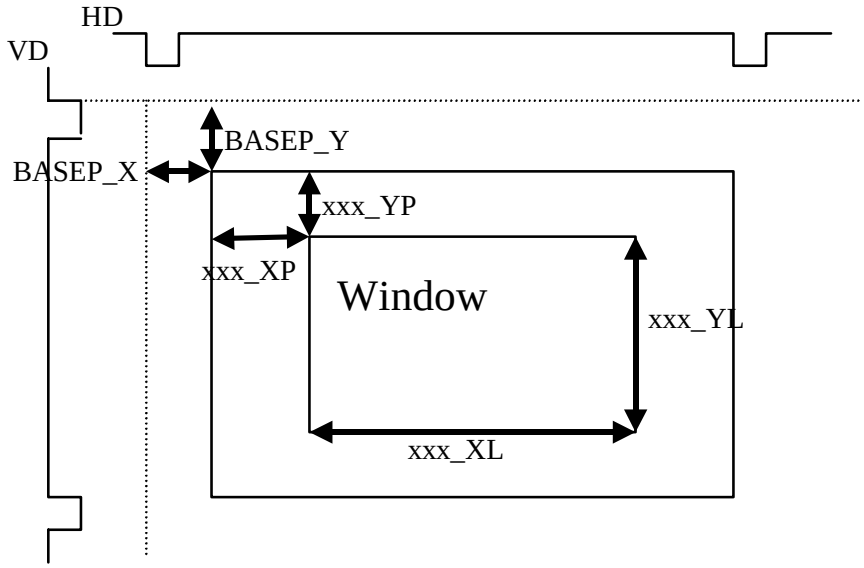


Figure 45: Window Setup

Window start position is specified with respect to the BASE_X, BASE_Y position (see BASEPX and BASEPY registers). Window start position in X-direction and window width is specified in units of pixels. Window start position in Y-direction and window height is specified in units of field lines. The *Table 21* shows the register used for window positioning.

Window positioning registers	Window
VIDWIN0XP VIDWIN0YP VIDWIN0XL VIDWIN0YL	Video Window 0 start position and size registers
VIDWIN1XP VIDWIN1YP VIDWIN1XL VIDWIN1YL	Video Window 1 start position and size registers
OSDWIN0XP OSDWIN0YP OSDWIN0XL OSDWIN0YL	OSD Bitmap Window 0 start position and size registers
OSDWIN1XP OSDWIN1YP OSDWIN1XL OSDWIN1YL	OSD Bitmap Window 1 / Attribute Window start position and size registers
CURXP CURYP CURXL CURYL	Hardware cursor start position and size registers

Table 21: Window positioning registers

4.6.3 Window Mode

4.6.3.1 Field / Frame Mode

Each video and bitmap window has two display modes: field mode and frame mode. The video encoder reads data from the video, bitmap windows with the help of two fields, even field and odd field. When the window mode is field mode, each line is duplicated in both even field as well as odd field. When window mode is frame mode, the even field reads every even line and the odd field reads every odd line. This relationship is shown in the Figure 46 and Figure 47.

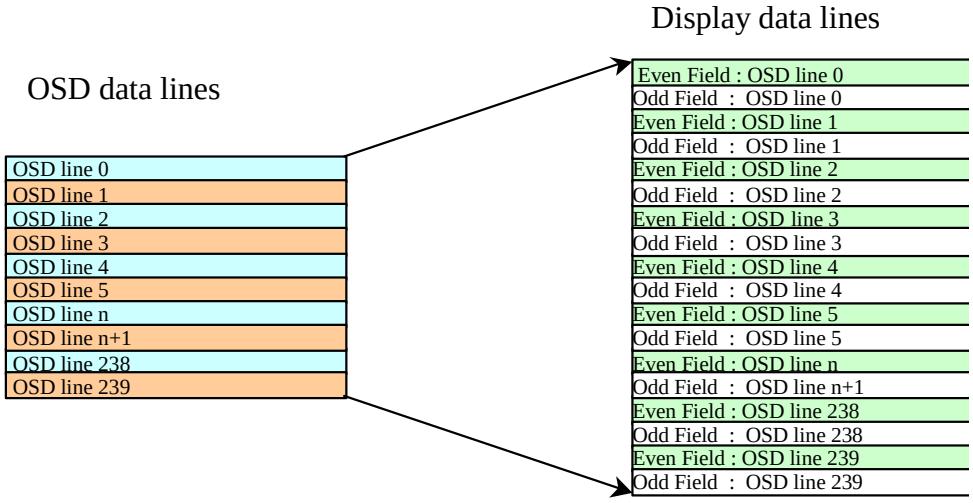


Figure 46: Window Field Mode

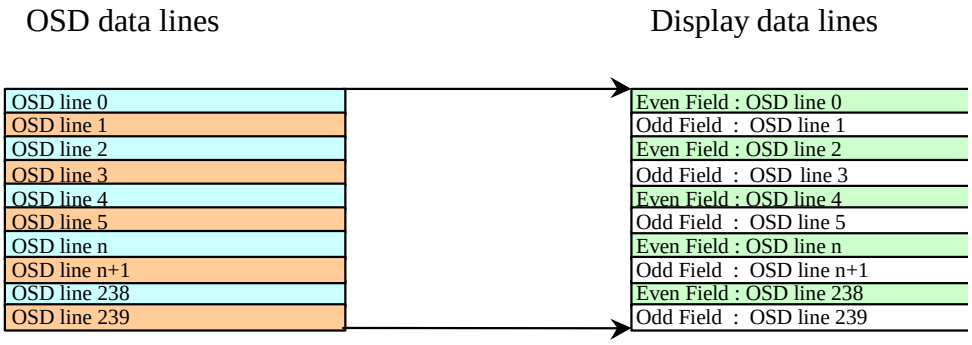


Figure 47: Window Frame Mode

4.6.3.2 Window Zooming

The vieo windows and OSD Bitmap windows can be zoomed along their horizontal and vertical directions by a factor of 2 or 4. *Figure 48* shows the zoom process and the parameters that must be setup to execute a zoom. Below are the steps involved in this procedure,

- Set the starting SDRAM address of the area desired to be magnified, offset, zoom factor and the display window size. The OSD will take data, starting from the start address, to generate a magnified image that fits into the display window.
- The offset is always the number of bursts in one horizontal line of SDRAM pixel data.
- Set the display position to the desired position of the window. Set the display height and display width to the desired magnified height and width.
- When zoom is enabled SDRAM data starting from the SDRAM start position will be magnified to fit into the display area specified by the display height and display width. For example, if the horizontal and vertical directions are set to 2x zoom and the display width and height are set 640x480, then a 320x240 block of data starting from the SDRAM start position will be magnified to 640x480 in the display window.

All of the registers used in the zoom process, are latched by the VD signal. So they can be safely updated any time, without any distortion.

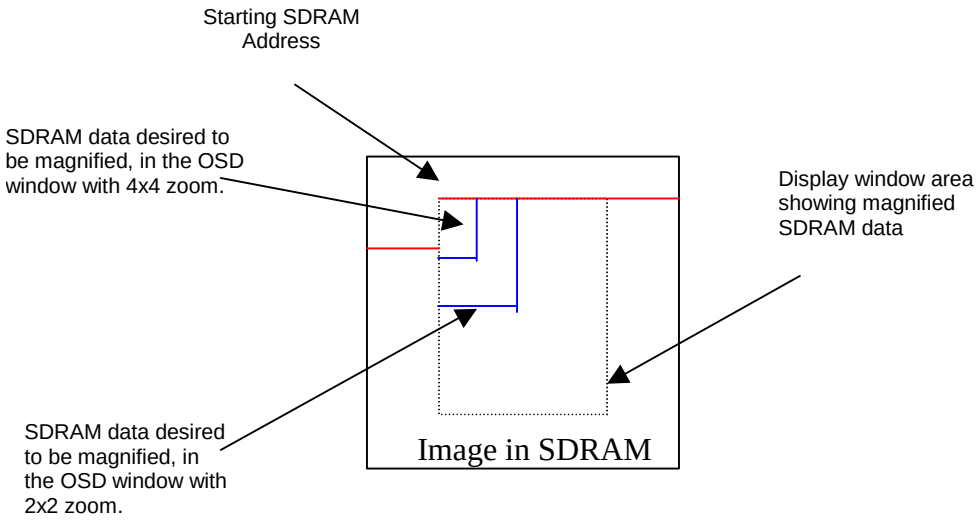


Figure 48: OSD Zoom Process

4.7 Bitmap Window

Bitmap window allows the user to display graphics and icons on the display unit. Bitmap Window 0 can only be used as a bitmap window. Bitmap Window 1 can be used as either bitmap window or attribute window. These windows can also display RGB16 data. The bitmap window uses a color lookup table (CLUT) in order to display a color for a given bitmap pixel value. A total of 256 colors are available. The maximum width of bitmap pixel is thus 8-bit. However 1,2,4-bit bitmaps are also supported. See section 4.5 for SDRAM storage format of bitmap data.

4.7.1 RGB16 data

In addition to bitmaps OSD bitmap windows can display RGB16 data also. Only one of the OSD bitmap windows can be set to display RGB16 data. Video Window 0 and 1 should not overlap with the OSD window if the window is set to RGB 16 mode.

4.7.2 Color Lookup Table

The user has the option to select either the ROM CLUT or can configure a RAM color look table.

4.7.2.1 ROM color look up table

The ROM CLUT is embedded into the internal ROM in OSD.

The ROM color look-up table values are given in Figure 49.

The color look-up chart is illustrated in Figure 50.

Addr	Y	Cb	Cr
0	255	128	128
1	249	102	132
2	243	77	136
3	238	52	140
4	232	26	145
5	226	0	149
6	225	145	149
7	219	119	154
8	213	94	158
9	208	68	162
10	202	43	166
11	196	17	170
12	195	162	171
13	189	136	175
14	183	111	179
15	178	85	183
16	172	60	187
17	166	34	191
18	165	179	192
19	159	153	196
20	154	128	200
21	148	102	204
22	142	77	209
23	136	51	213
24	135	196	213
25	129	170	218
26	124	145	222
27	118	119	226
28	112	94	230
29	106	68	234
30	105	212	235
31	100	187	239
32	94	161	243
33	88	136	247
34	82	110	251
35	76	85	255
36	240	137	102
37	234	111	107
38	228	86	111
39	222	60	115
40	216	35	119
41	211	9	123
42	210	154	124
43	204	128	128
44	198	102	132
45	192	77	136
46	187	52	140
47	181	26	145
48	180	170	145
49	174	145	149
50	168	119	154
51	162	94	158
52	157	68	162
53	151	43	166
54	150	187	167
55	144	162	171
56	138	136	175
57	132	111	179
58	127	85	183
59	121	60	187
60	120	204	188
61	114	179	192
62	108	153	196

Addr	Y	Cb	Cr
64	97	102	204
65	91	77	209
66	90	221	209
67	84	196	213
68	78	170	218
69	73	145	222
70	67	119	226
71	61	94	230
72	225	145	77
73	219	120	81
74	213	94	85
75	207	69	89
76	201	43	94
77	195	18	98
78	195	162	98
79	189	137	102
80	183	111	107
81	177	86	111
82	171	60	115
83	165	35	119
84	165	179	120
85	159	154	124
86	153	128	128
87	147	102	132
88	141	77	136
89	136	52	140
90	135	196	141
91	129	170	145
92	123	145	149
93	117	119	154
94	111	94	158
95	106	68	162
96	105	213	162
97	99	187	167
98	93	162	171
99	87	136	175
100	81	111	179
101	76	85	183
102	75	230	184
103	69	204	188
104	63	179	192
105	57	153	196
106	52	128	200
107	46	102	204
108	209	154	52
109	203	128	56
110	198	103	60
111	192	77	64
112	186	52	68
113	180	26	72
114	179	171	73
115	174	145	77
116	168	120	81
117	162	94	85
118	156	69	89
119	150	43	94
120	149	188	94
121	144	162	98
122	138	137	102
123	132	111	107
124	126	86	111
125	120	60	115
126	119	204	116

Addr	Y	Cb	Cr
128	108	154	124
129	102	128	128
130	96	102	132
131	90	77	136
132	90	221	137
133	84	196	141
134	78	170	145
135	72	145	149
136	66	119	154
137	60	94	158
138	60	238	158
139	54	213	162
140	48	187	167
141	42	162	171
142	36	136	175
143	30	111	179
144	194	162	26
145	188	137	30
146	182	111	34
147	177	86	38
148	171	60	43
149	165	35	47
150	164	179	47
151	158	154	52
152	152	128	56
153	147	103	60
154	141	77	64
155	135	52	68
156	134	196	69
157	128	171	73
158	123	145	77
159	117	120	81
160	111	94	85
161	105	69	89
162	104	213	90
163	98	188	94
164	93	162	98
165	87	137	102
166	81	111	107
167	75	86	111
168	74	230	111
169	68	204	116
170	63	179	120
171	57	154	124
172	51	128	128
173	45	102	132
174	44	247	133
175	39	221	137
176	33	196	141
177	27	170	145
178	21	145	149
179	15	119	154
180	179	171	0
181	173	146	5
182	167	120	9
183	161	95	13
184	155	69	17
185	150	44	21
186	149	188	22
187	143	162	26
188	137	137	30
189	131	111	34
190	126	86	38

Addr	Y	Cb	Cr
192	119	205	43
193	113	179	47
194	107	154	52
195	101	128	56
196	96	103	60
197	90	77	64
198	89	222	65
199	83	196	69
200	77	171	73
201	72	145	77
202	66	120	81
203	60	94	85
204	59	239	86
205	53	213	90
206	47	188	94
207	42	162	98
208	36	137	102
209	30	111	107
210	29	255	107
211	23	230	111
212	17	204	116
213	12	179	120
214	6	154	124
215	71	88	247
216	66	91	238
217	56	96	222
218	51	99	213
219	41	105	196
220	36	108	188
221	25	114	170
222	20	117	162
223	10	122	145
224	5	125	136
225	140	49	28
226	130	55	35
227	110	66	50
228	100	72	57
229	80	83	71
230	70	89	78
231	50	100	92
232	40	105	100
233	20	117	114
234	10	122	121
235	27	247	109
236	25	238	110
237	21	222	113
238	19	213	114
239	16	196	117
240	14	188	118
241	10	170	121
242	8	162	122
243	4	145	125
244	2	136	127
245	238	128	128
246	221	128	128
247	187	128	128
248	170	128	128
249	136	128	128
250	119	128	128
251	85	128	128
252	68	128	128
253	34	128	128
254	17	128	128

63	103	128	200	127	114	179	120	191	120	60	43	255	0	128	128

Figure 49: ROM CLUT Color values (Each Y, Cb or Cr value is represented in decimal number)

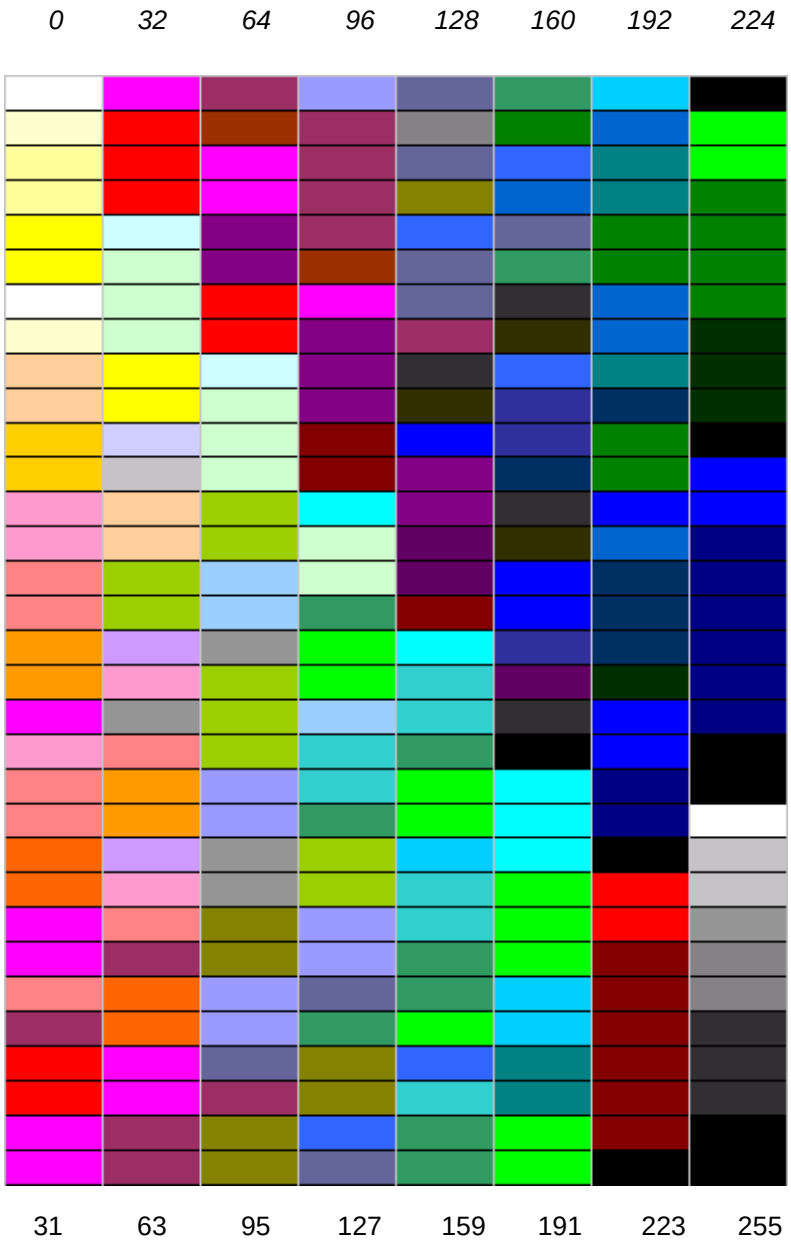


Figure 50: ROM CLUT Color Chart

4.7.2.2 RAM Color Lookup Table

A RAM CLUT can be used instead of the default ROM CLUT, which has to be written by the user into the internal OSD RAM memory.

To setup the OSD RAM CLUT, following steps are required:

Wait for the CPBSY bit of register *MISCCTL* to be zero

Write the address and the value of Cr into the CLUTRAMYCB register. The address is the offset address in the OSD RAM for 1 set of Y, Cb and Cr values.

Write Y and Cb value into the *MISCCTL* register

Repeat the previous steps until the RAM table is loaded completely.

Note: After a device reset, the color values of the RAM CLUT are undetermined.

Sample code to write to RAM CLUT is given below.

```
extern Uint8 lutY[255];          //LUT entries for Y (0-255)
extern Uint8 lutCb[255];         //LUT entries for Cb (0-255)
extern Uint8 lutCr[255];         //LUT entries for Cr (0-255)
Uint8 i;
for(i=0; i< 255; i++) {
       while(OSD_FGET( MISCCTL, CPBSY) );
       OSD_RSET(CLUTRAMCR,  ((Uint16)Cr[i] << 8) | i;
       // Write the LUT address and Cr value
       OSD_RSET(CLUTRAMYCB, ((Uint16)Y[i] << 8) | (Uint16)Cb[i];
       // Write  LUT values from Y, Cb arrays
}
```

4.7.2.3 Selecting RAM/ROM CLUT

Selection between RAM and ROM CLUT can be done separately for OSD Bitmap Window 0, OSD Bitmap Window 1. For OSD Bitmap Window 0 configure CLUTS0 bit in register *OSDWIN0MD.* For OSD Bitmap Window 1 configure CLUTS1 bit in register *OSDWIN1MD.*

4.7.2.4 1,2,4-bit Bitmap and CLUT

When the bitmap size is 1,2 or 4-bit, the registers *W0BMP01 to W0BMPEF* or W1BMP01 to W1BMPEF can be used to map any of the 256 colors to a bitmap value. For example, for 1-bit bitmap data, any of the 256 colors in the CLUT can be mapped to bit value “0” and any of the 256 colors can be mapped to bit value “1”. This mapping can be specified separately for each OSD Bitmap window. The *Table: 22* shows the register, which can be used to select the color for a bitmap value.

Register : Field (x = 0,1 for OSD Bitmap Window 0,1 respectively)	**4-bit bitmap** Color corresponding to bitmap value	**2-bit bitmap** Color corresponding to bitmap value	**1-bit bitmap** Color corresponding to bitmap value
WxBMP01 : PAL00	0	0	0
WxBMP01 : PAL01	1	-	-
WxBMP23 : PAL02	2	-	-
WxBMP23 : PAL03	3	-	-
WxBMP45 : PAL04	4	-	-
WxBMP45 : PAL05	5	1	-
WxBMP67 : PAL06	6	-	-
WxBMP67 : PAL07	7	-	-
WxBMP89 : PAL08	8	-	-
WxBMP89 : PAL09	9	-	-
WxBMPAB : PAL10	10	2	-
WxBMPAB : PAL11	11	-	-
WxBMPCD : PAL12	12	-	-
WxBMPCD : PAL13	13	-	-
WxBMPEF : PAL14	14	-	-
WxBMPEF : PAL15	15	3	1

Table: 22 1,2,4-bit Bitmap Color Selection

4.7.3 Blending and Transparency

OSD supports transparency mode with bitmap windows. If transparency is enabled, then any pixel on the bitmap display that has a value of 0 will allow video to be displayed. In this case, blending factor would be applied before displaying the video. Essentially, 0 valued pixels are considered transparent, and the background color (after blending) will show through the bitmap. Background color selection and Cb/Cr format selection can be done in the *OSDMODE* register.

OSD also supports color blending at the pixel level. This feature is available for the bitmap windows only. If the window color blending is enabled, the amount of blending of each pixel is determined by the blending factor. The different blending factors are shown in Table 23.

Blending factor and transparency is configured using *OSDWIN0MD* and *OSDWIN1MD* registers for OSD Bitmap window 0 and 1 respectively.

Transparency	Blending Factor	OSD Window contribution	Video contribution
OFF	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
ON		If pixel value = 0	
	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
		If pixel value != 0	
	X	1	0

Table 23: Bending and Transparency in OSD

4.7.4 Attribute Window

OSD bitmap window 1 can be configured as an attribute window. The attribute window allows blending and blinking of individual pixels in the display windows. In particular the attribute window allows to:

Blend pixels from OSD Window 0 with Video Window 0 or Video Window 1

Blink pixels in OSD Window 0

The SDRAM start address, position, and size of the attribute window needs to be configured. However, the data in SDRAM is interpreted as shown in Figure 51. Bit3 specifies whether or not to blink the corresponding pixel and Bit2-Bit0 specifies the blending factor to be applied to the corresponding pixel. The blending factors are defined in Table 23.

Bit 3	Bit 2	Bit 1	Bit 0
0 - No blink 1 - Blink	Blend Factor		

Figure 51: Attribute Data Format

As shown in Figure 52 the attribute window applies blending and blinking to OSD window 0 depending on the position of the attribute window.

Attribute window is configured using register *OSDATRMD*

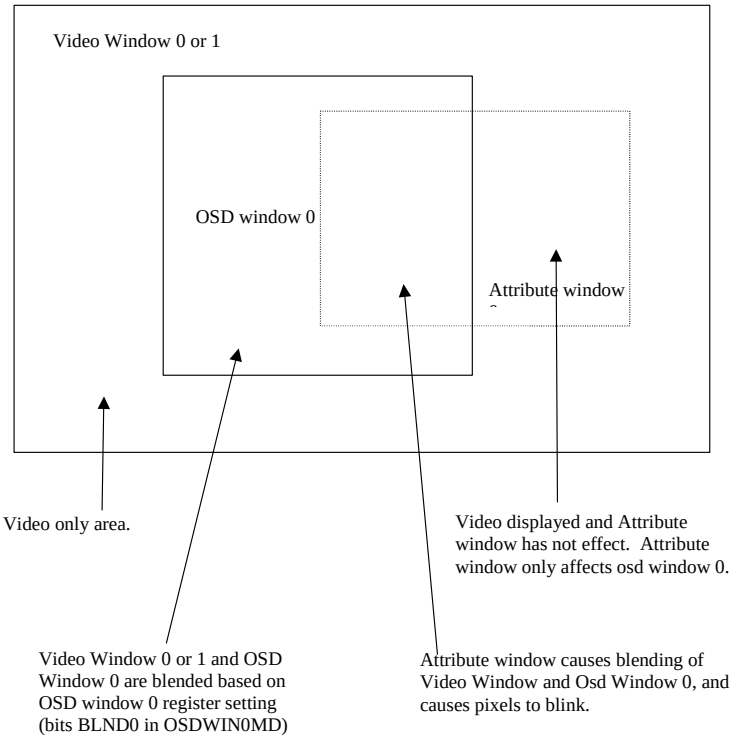


Figure 52:The Attribute Window's Relationship to the Other Windows

4.8 Rectangular Hardware Cursor

The rectangular hardware cursor always appears on top of other OSD Windows. The cursor's size, color, horizontal and vertical thickness can be specified. This cursor can also be configured to use the ROM or RAM CLUT.

Figure 53 shows an example usage of the rectangle cursor. Yellow Line shows the rectangle cursor and ICON1-4 are displayed by using OSD window 0 or1.

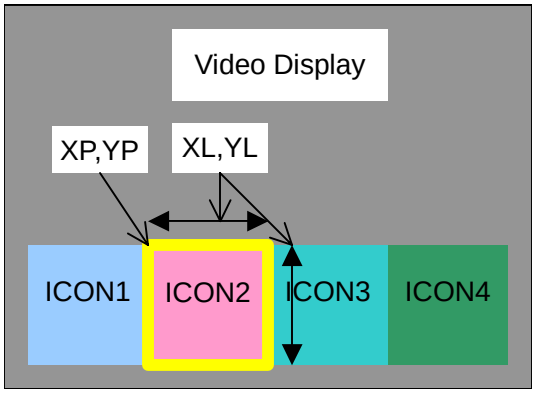


Figure 53: Rectangular Cursor

Register	Description
RECTCUR	Controls the size and enable / disable rectangular cursor.
CURXP	Sets the horizontal display start position
CURYP	Sets the vertical display start position
CURXL	Sets the horizontal display width in pixels.
CURYL	Sets the vertical display height in pixels/lines

4.9 Window Expansion (VGA to NTSC/PAL Conversion)

OSD supports conversion from VGA size image to NTSC/PAL image during display of video windows, bitmap windows. *Table 24* shows the expansion ratios supported.

	Horizontal	Vertical
Video Window	9/8	6/5
Bitmap Window	--	6/5

Table 24: Window Expansion

For Video Windows horizontal 9/8 expansion is enabled by VHRSZ bit and vertical 6/5 expansion is enabled by VVRSZ bit of *OSDMODE* register. When either of them is enabled, the Expansion Filter can be applied by EF bit of the same register.

For Bitmap Window, horizontal 9/8 expansion is enabled by OHRSZ bit and vertical 6/5 expansion is enabled by OVRSZ bit of *OSDMODE* register.

4.10 OSD Ping Pong Buffer

The main video window (video window 0) supports ping-pong buffers. Initially the SDRAM source address for OSD Video window 0 can be set to the SDRAM address specified in *VIDWINADH and VIDWIN0ADL* registers, and when the ping pong buffer toggle bit is cleared the SDRAM source address switches to the address specified in *PPVWIN0ADH and PPVWIN0ADH* registers. Ping Pong buffer switching is done by configuring PPSW bit in *MISCCTL* register. The buffer switching is illustrated Figure 54.

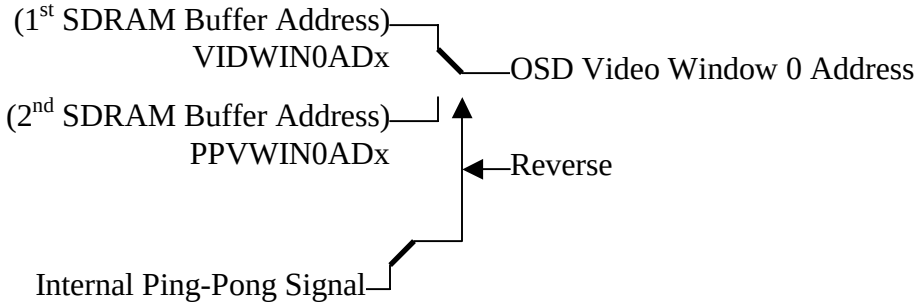


Figure 54: Ping-Pong buffers for the main video window (OSD Video Window 0)

4.11 On Screen Display Register Map (OSD)

Address	Register	Description
0003:0680	OSDMODE	OSD Mode Setup
0003:0682	VIDWINMD	Video Window Mode Setup
0003:0684	OSDWIN0MD	OSD Window 0 Mode Setup
0003:0686	OSDWIN1MD	OSD Window 1 Mode Setup
0003:0686	OSDATRMD	OSD Attribute Window Mode Setup
0003:0688	RECTCUR	Rectangular Cursor Setup
0003:068A	RSV0	Reserved
0003:068C	VIDWIN0OFST	Video Window 0 Offset
0003:068E	VIDWIN1OFST	Video Window 1 Offset
0003:0690	OSDWIN0OFST	OSD Window 0 Offset
0003:0692	OSDWIN1OFST	OSD Window 1 Offset
0003:0694	VIDWINADH	Video Window 0/1 Address - High
0003:0696	VIDWIN0ADL	Video Window 0 Address - Low
0003:0698	VIDWIN1ADL	Video Window 1 Address - Low
0003:069A	OSDWINADH	OSD Window 0/1 Address - High
0003:069C	OSDWIN0ADL	OSD Window 0 Address - Low
0003:069E	OSDWIN1ADL	OSD Window 1 Address - Low
0003:06A0	BASEPX	Base Pixel X
0003:06A2	BASEPY	Base Pixel Y
0003:06A4	VIDWIN0XP	Video Window 0 X-Position
0003:06A6	VIDWIN0YP	Video Window 0 Y-Position
0003:06A8	VIDWIN0XL	Video Window 0 X-Size
0003:06AA	VIDWIN0YL	Video Window 0 Y-Size
0003:06AC	VIDWIN1XP	Video Window 1 X-Position
0003:06AE	VIDWIN1YP	Video Window 1 Y-Position
0003:06B0	VIDWIN1XL	Video Window 1 X-Size
0003:06B2	VIDWIN1YL	Video Window 1 Y-Size

0003:06B4	OSDWIN0XP	OSD Bitmap Window 0 X-Position
0003:06B6	OSDWIN0YP	OSD Bitmap Window 0 Y-Position
0003:06B8	OSDWIN0XL	OSD Bitmap Window 0 X-Size
0003:06BA	OSDWIN0YL	OSD Bitmap Window 0 Y-Size
0003:06BC	OSDWIN1XP	OSD Bitmap Window 1 X-Position
0003:06BE	OSDWIN1YP	OSD Bitmap Window 1 Y-Position
0003:06C0	OSDWIN1XL	OSD Bitmap Window 1 X-Size
0003:06C2	OSDWIN1YL	OSD Bitmap Window 1 Y-Size
0003:06C4	CURXP	Rectangular Cursor Window X-Position
0003:06C6	CURYP	Rectangular Cursor Window Y-Position
0003:06C8	CURXL	Rectangular Cursor Window X-Size
0003:06CA	CURYL	Rectangular Cursor Window Y-Size
0003:06CC	RSV1	Reserved
0003:06CE	RSV2	Reserved
0003:06D0	W0BMP01	Window 0 Bitmap Value to Palette Map 0/1
0003:06D2	W0BMP23	Window 0 Bitmap Value to Palette Map 2/3
0003:06D4	W0BMP45	Window 0 Bitmap Value to Palette Map 4/5
0003:06D6	W0BMP67	Window 0 Bitmap Value to Palette Map 6/7
0003:06D8	W0BMP89	Window 0 Bitmap Value to Palette Map 8/9
0003:06DA	W0BMPAB	Window 0 Bitmap Value to Palette Map A/B
0003:06DC	W0BMPCD	Window 0 Bitmap Value to Palette Map C/D
0003:06DE	W0BMPEF	Window 0 Bitmap Value to Palette Map E/F
0003:06E0	W1BMP01	Window 1 Bitmap Value to Palette Map 0/1
0003:06E2	W1BMP23	Window 1 Bitmap Value to Palette Map 2/3
0003:06E4	W1BMP45	Window 1 Bitmap Value to Palette Map 4/5
0003:06E6	W1BMP67	Window 1 Bitmap Value to Palette Map 6/7
0003:06E8	W1BMP89	Window 1 Bitmap Value to Palette Map 8/9
0003:06EA	W1BMPAB	Window 1 Bitmap Value to Palette Map A/B
0003:06EC	W1BMPCD	Window 1 Bitmap Value to Palette Map C/D
0003:06EE	W1BMPEF	Window 1 Bitmap Value to Palette Map E/F
0003:06F0	RSV3	Reserved
0003:06F2	RSV4	Reserved
0003:06F4	MISCCTL	Miscellaneous Control
0003:06F6	CLUTRAMYCB	CLUT RAM Y/Cb Setup
0003:06F8	CLUTRAMCR	CLUT RAM Cr/Mapping Setup
0003:06FA	RSV5	Reserved
0003:06FC	PPVWIN0ADH	Ping-Pong Video Window 0 Address (High)
0003:06FE	PPVWIN0ADL	Ping-Pong Video Window 0 Address (Low)

4.12 On Screen Display Registers

4.12.1 OSDMODE

OSD Mode Setup

OSDMODE 0003:0680 offset: 0x00 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS	OVRSZ	OHRSZ	EF	VVRSZ	VHRSZ	FSINV	CLUT	CABG[7]	CABG[6]	CABG[5]	CABG[4]	CABG[3]	CABG[2]	CABG[1]	CABG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	CS	0	R/W	Cb/Cr or Cr/Cb format » 0: Cb/Cr « » 1: Cr/Cb «
14	OVRSZ	0	R/W	OSD Window Vertical Expansion Enable » 0: x 1 « » 1: x 6/5 « When enabled, the bitmap window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640x480) image on a PAL television (720x576); i.e., 480 x 6/5=576
13	OHRSZ	0	R/W	OSD Window Horizontal Expansion Enable » 0: x 1 « » 1: x 9/8 « When enabled, the bitmap window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640x480) image on a PAL / NTSC television (720); i.e., 640 x 9/8=720
12	EF	0	R/W	Expansion Filter Enable » 0: Off « » 1: On « Valid when either VVRSZ or VHRSZ is on, or video window zoom is set. Caution is required when using the filter since expansion filter memory can only correspond to 720 horizontal pixels. **This bit is latched by VD.*
11	VVRSZ	0	R/W	Video Window Vertical Expansion Enable » 0: x 1 « » 1: x 6/5 « When enabled, the video window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640x480) image on a PAL television (720x576); i.e., 480 x 6/5=576 **This bit is latched by VD.*

10	VHRSZ	0	R/W	Video Window Horizontal Expansion Enable » 0: x 1 « » 1: x 9/8 « When enabled, the video window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640x480) image on an NTSC/PAL television (720x576); i.e., 640 x 9/8 = 720 **This bit is latched by VD.*
9	FSINV	0	R/W	Field signal inversion » 0: Uninverted « » 1: Inverted « **This bit is latched by VD.*
8	CLUT	0	R/W	CLUT selection Selects look-up table » 0: ROM « » 1: RAM « **This bit is latched by VD.*
7:0	CABG	0	R/W	Background Color CLUT Specifies image display background color by CLUT address. In parts that do not display image, color specified by this register is displayed.

4.12.2 VIDWINMD

Video Window Mode Setup

VIDWINMD 0003:0682 offset: 0x02 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VFINV	V1EFC	VHZ1[1]	VHZ1[0]	VVZ1[1]	VVZ1[0]	VFF1	ACT1	RSV	V0EFC	VHZ0[1]	VHZ0[0]	VVZ0[1]	VVZ0[0]	VFF0	ACT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	VFINV	0	R/W	Video window 0/1 Expansion filter co-efficient Inverse » 0: Normal « » 1: Inversed « Note: If V1EFC or V0EFC is set, this bit is valid
14	V1EFC	0	R/W	Video window 1 Expansion filter co-efficient » 0: same co-eficients for field-0 and field-1 « » 1: different co-eficients for field-0 and field-1 « Valid when vertical expansion and expansion filter is set.
13:12	VHZ1	0	R/W	Video window1 horizontal direction zoom » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.
11:10	VVZ1	0	R/W	Video window1 vertical direction zoom » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.
9	VFF1	0	R/W	Video window1 display mode » 0: Field mode « » 1: Frame mode « *This bit is latched by VD.
8	ACT1	0	R/W	Sets image display on/off video window1 » 0: Off « » 1: On « *This bit is latched by VD.
7	RSV			Reserved
6	V0EFC	0	R/W	Video window 0 Expansion filter co-efficient » 0: same co-eficients for field-0 and field-1 « » 1: different co-eficients for field-0 and field-1 « Valid when vertical expansion and expansion filter is set.
5:4	VHZ0	0	R/W	Video window0 horizontal direction zoom » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.
3:2	VVZ0	0	R/W	Video window0 vertical direction zoom » 0: x1 « » 1: x2 « » 0: x4 « » 1: Reserved (same as '00') « *This bit is latched by VD.
1	VFF0	0	R/W	Video window0 display mode » 0: Field mode « » 1: Frame mode « *This bit is latched by VD.
0	ACT0	0	R/W	Sets image display on/off video window0 » 0: Off « » 1: On « *This bit is latched by VD.

4.12.3 OSDWIN0MD

OSD Window 0 Mode Setup

OSDWIN0MD 0003:0684 offset: 0x04 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	ATN0E	RGB0E	CLUTS0	OHZ0[1]	OHZ0[0]	OVZ0[1]	OVZ0[0]	BMW0[1]	BMW0[0]	BLND0[2]	BLND0[1]	BLND0[0]	TE0	OFF0	OACT0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14	ATN0E	0	R/W	Attenuation Enable for REC601 » 0: Normal (Y: 0-255, Cr: 0-255, Cb: 0-255) « » 1: Attenuated (Y: 16-235, Cr: 16-240, Cb: 16-240) «
13	RGB0E	0	R/W	RGB input for window 0 Enable » 0: bitmap input « » 1: 16-bit RGB mode « Only one OSD window can be configured for RGB input mode
12	CLUTS0	0	R/W	CLUT select » 0: ROM-look-up table « » 1: RAM-look-up table « *This bit is latched by VD.
11:10	OHZ0	0	R/W	OSD Window0 Horizontal Zoom » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.
9:8	OVZ0	0	R/W	OSD Window0 Vertical Zoom » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.
7:6	BMW0	0	R/W	Bitmap bit width for OSD window0 » 00: 1 « » 01: 2 « » 10: 4 « » 11: 8 « *This bit is latched by VD, Valid for bitmap input mode
5:3	BLND0	0	R/W	Blending Ratio for OSD Window0 and Video Window 0/1 OSD Video » 000: 0 1 « » 001: 1/8 7/8 « » 010: 2/8 6/8 « » 011: 3/8 5/8 « » 100: 4/8 4/8 « » 101: 5/8 3/8 « » 110: 6/8 2/8 « » 111: 1 0 « *This bit is latched by VD.
2	TE0	0	R/W	Transparency Enable for OSD Window0 » 0: disable « » 1: enable « In Bitmap mode, When transparency is on, blending is only performed for pixels whose bitmap value is 0. In RGB mode, if transparency is on, the pixels with RGB as 0x0000 is blended with video windows. The blending is done as per the BLND0 register configuration. *This bit is latched by VD.
1	OFF0	0	R/W	OSD Window0 Display Mode » 0: Field mode « » 1: Frame mode « *This bit is latched by VD.
0	OACT0	0	R/W	OSD Window0 Active (displayed) » 0: Off « » 1: On « *This bit is latched by VD.

4.12.4 OSDWIN1MD

OSD Window 1 Mode Setup

OSDWIN1MD 0003:0686 offset: 0x06 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OASW	ATN1E	RGB1E	CLUTS1	OHZ1[1]	OHZ1[0]	OVZ1[1]	OVZ1[0]	BMW1[1]	BMW1[0]	BLND1[2]	BLND1[1]	BLND1[0]	TE1	OFF1	OACT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	OASW	0	R/W	OSD Window1 Attribute Mode Enable » 0: OSD Window1 « » 1: Attribute window « *This bit is latched by VD.
14	ATN1E	0	R/W	Attenuation Enable for REC601 » 0: Normal (Y: 0-255, Cr: 0-255, Cb: 0-255) « » 1: Attenuated (Y: 16-235, Cr: 16-240, Cb: 16-240) «
13	RGB1E	0	R/W	RGB input for window 1 Enable » 0: bitmap input« » 1: 16-bit RGB mode « Only one OSD window can be configured for RGB input mode
12	CLUTS1	0	R/W	CLUT Select OASW=0 » 0: ROM-look-up table « » 1: RAM-look-up table «
11:10	OHZ1	0	R/W	OSD Window1 Horizontal Zoom OASW=0 » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved « *This bit is latched by VD.
9:8	OVZ1	0	R/W	OSD Window1 Vertical Zoom OASW=0 » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved « *This bit is latched by VD.
7:6	BMW1	0	R/W	Bitmap Bit Width OASW=0 Bitmap bit width for OSD Window1 » 00: 1-bit « » 01: 2-bits « » 10: 4-bits « » 11: 8-bits « *This bit is latched by VD, Valid for bitmap input mode
5:3	BLND1	0	R/W	Blending Ratio for OSD Window1(OASW=0) & Video Window 0/1 OSD Video » 000: 0 1 « » 001: 1/8 7/8 « » 010: 2/8 6/8 « » 011: 3/8 5/8 « » 100: 4/8 4/8 « » 101: 5/8 3/8 « » 110: 6/8 2/8 « » 111: 1 0 « *This bit is latched by VD.
2	TE1	0	R/W	Transparency Enable for OSD Window0 OASW=0 » 0: disable « » 1: enable « In Bitmap mode, When transparency is on, blending is only performed for pixels whose bitmap value is 0. In RGB mode, if transparency is on, the pixels with RGB as 0x0000 is blended with video windows. The blending is done as per the BLND1 register configuration. *This bit is latched by VD.
1	OFF1	0	R/W	OSD Window0 Display Mode OASW=0 » 0: Field mode « » 1: Frame mode « *This bit is latched by VD.
0	OACT1	0	R/W	OSD Window0 Active (displayed) OASW=0 » 0: Off « » 1: On « *This bit is latched by VD.

4.12.5 OSDATRMD

OSD Attribute Window Mode Setup

OSDATRMD 0003:0686 offset: 0x06 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OASW	RSV	RSV	NA1	OHZA[1]	OHZA[0]	OVZA[1]	OVZA[0]	BLNKINT[1]	BLNKINT[0]	NA2[2]	NA2[1]	NA2[0]	NA3	OFFA	BLNK
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	OASW	0	R/W	OSD Window1 Attribute Mode Enable » 0: OSD Window1 « » 1: Attribute window « Note: This bit enables attribute mode for OSD Window1. *This bit is latched by VD.*
14:13	RSV			Reserved
12	NA1	0	R/W	Not Applicable in Attribute Window **OASW=1** Not Used, Please set to 0 *This bit is latched by VD.*
11:10	OHZA	0	R/W	OSD Attribute Window Horizontal Zoom **OASW=1** » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.*
9:8	OVZA	0	R/W	OSD Window1 or Attribute Window Vertical Zoom **OASW=1** » 00: x1 « » 01: x2 « » 10: x4 « » 11: Reserved (same as '00') « *This bit is latched by VD.*
7:6	BLNKINT	0	R/W	Blinking Interval **OASW=1** » 00: 1-unit « » 01: 2-units « » 10: 3-units « » 11: 4-units « Specifies the blinking interval of the attribute window in units of 8 VD pulses *This bit is latched by VD.*
5:3	NA2	0	R/W	Not Applicable in Attribute Window **OASW=1** Not Used, Please set to 0 *This bit is latched by VD.*
2	NA3	0	R/W	Not Applicable in Attribute Window OASW=1 Not Used, Please set to 0 *This bit is latched by VD.
1	OFFA	0	R/W	OSD Attribute Window Display Mode **OASW=1** » 0: Field mode « » 1: Frame mode « *This bit is latched by VD.*
0	BLNK	0	R/W	OSD Attribute Window Blink Enable **OASW=1** » 0: disable « » 1: enable « *This bit is latched by VD.*

4.12.6 RECTCUR

Rectangular Cursor Setup

RECTCUR 0003:0688 offset: 0x08 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RCAD[7]	RCAD[6]	RCAD[5]	RCAD[4]	RCAD[3]	RCAD[2]	RCAD[1]	RCAD[0]	CLUTSR	RCHW[2]	RCHW[1]	RCHW[0]	RCVW[2]	RCVW[1]	RCVW[0]	RCACT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RCAD	0	R/W	Rectangular Cursor Color Palette Address
7	CLUTSR	0	R/W	CLUT Select » 0: ROM-look-up table « » 1: RAM-look-up table « **This bit is latched by VD.*
6:4	RCHW	0	R/W	Rectangular Cursor Horizontal Line Width Width is 4xRCHW, with 0 interpreted as 1 pixel Range is: 1,4,8,16,20,24,28 pixels **This bit is latched by VD.*
3:1	RCVW	0	R/W	Rectangular Cursor Vertical Line Width Width is 2xRCVW, with 0 interpreted as 1 line Range is: 1,2,4,6,8,10,12,14 lines **This bit is latched by VD.*
0	RCACT	0	R/W	Rectangular Cursor Active (displayed) » 0: Off « » 1: On « **This bit is latched by VD.*

4.12.7 VIDWIN0OFST

Video Window 0 Offset

VIDWIN0OFST 0003:068C offset: 0x0C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	V0LO[8]	V0LO[7]	V0LO[6]	V0LO[5]	V0LO[4]	V0LO[3]	V0LO[2]	V0LO[1]	V0LO[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Resereved
8:0	V0LO	0	R/W	Video Window 0 Line Offset Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16 i.e., 720/16 = 45 (0x2D) *Note: If line width setting for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.* **This bit is latched by VD.*

4.12.8 VIDWIN1OFST

Video Window 1 Offset

VIDWIN1OFST 0003:068E offset: 0x0E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	V1LO[8]	V1LO[7]	V1LO[6]	V1LO[5]	V1LO[4]	V1LO[3]	V1LO[2]	V1LO[1]	V1LO[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Resereved
8:0	V1LO	0	R/W	Video Window 1 Line Offset Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16 i.e., 720/16 = 45 (0x2D) *Note: If line width setting for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.* **This bit is latched by VD.*

4.12.9 OSDWIN0OFST

OSD Window 0 Offset

OSDWIN0OFST 0003:0690 offset: 0x10 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	O0LO[8]	O0LO[7]	O0LO[6]	O0LO[5]	O0LO[4]	O0LO[3]	O0LO[2]	O0LO[1]	O0LO[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Resereved
8:0	O0LO	0	R/W	OSD Window 0 Line Offset Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in pixels * bitdepth / 256-bits/burst i.e., 64*8/256 = 2 *Note: If line width and bitdepth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.* **This bit is latched by VD.*

4.12.10 OSDWIN1OFST

OSD Window 1 Offset

OSDWIN1OFST 0003:0692 offset: 0x12 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	O1LO[8]	O1LO[7]	O1LO[6]	O1LO[5]	O1LO[4]	O1LO[3]	O1LO[2]	O1LO[1]	O1LO[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Resereved
8:0	O1LO	0	R/W	OSD Window 1 Line Offset Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in pixels * bitdepth / 256-bits/burst i.e., 64*8/256 = 2 *Note: If line width and bitdepth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.* **This bit is latched by VD.*

4.12.11 VIDWINADH

Video Window 0/1 Address - High

VIDWINADH 0003:0694 offset: 0x14 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	V1AH[6]	V1AH[5]	V1AH[4]	V1AH[3]	V1AH[2]	V1AH[1]	V1AH[0]	RSV	V0AH[6]	V0AH[5]	V0AH[4]	V0AH[3]	V0AH[2]	V0AH[1]	V0AH[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	V1AH	0	R/W	Video Window 1 SDRAM Source Address - High 7 MSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*
7	RSV			Reserved
6:0	V0AH	0	R/W	Video Window 0 SDRAM Source Address - High 7 MSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*

4.12.12 VIDWIN0ADL

Video Window 0 Address - Low

VIDWIN0ADL 0003:0696 offset: 0x16 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	V0AL[15]	V0AL[14]	V0AL[13]	V0AL[12]	V0AL[11]	V0AL[10]	V0AL[9]	V0AL[8]	V0AL[7]	V0AL[6]	V0AL[5]	V0AL[4]	V0AL[3]	V0AL[2]	V0AL[1]	V0AL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	V0AL	0	R/W	Video Window 0 SDRAM Source Address - Low 16 LSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. *This bit is latched by VD.*

4.12.13 VIDWIN1ADL

Video Window 1 Address - Low

VIDWIN1ADL 0003:0698 offset: 0x18 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	V1AL[15]	V1AL[14]	V1AL[13]	V1AL[12]	V1AL[11]	V1AL[10]	V1AL[9]	V1AL[8]	V1AL[7]	V1AL[6]	V1AL[5]	V1AL[4]	V1AL[3]	V1AL[2]	V1AL[1]	V1AL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	V1AL	0	R/W	Video Window 1 SDRAM Source Address - Low 16 LSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. *This bit is latched by VD.*

4.12.14 OSDWINADH

OSD Window 0/1 Address - High

OSDWINADH 0003:069A offset: 0x1A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	O1AH[6]	O1AH[5]	O1AH[4]	O1AH[3]	O1AH[2]	O1AH[1]	O1AH[0]	RSV	O0AH[6]	O0AH[5]	O0AH[4]	O0AH[3]	O0AH[2]	O0AH[1]	O0AH[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	O1AH	0	R/W	OSD Window 1 / Attribute Window SDRAM Source Address - High 7 MSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units: of32 bytes. **This bit is latched by VD.*
7	RSV			Reserved
6:0	O0AH	0	R/W	OSD Window 0 SDRAM Source Address - High 7 MSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*

4.12.15 OSDWIN0ADL

OSD Window 0 Address - Low

OSDWIN0ADL 0003:069C offset: 0x1C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O0AL[15]	O0AL[14]	O0AL[13]	O0AL[12]	O0AL[11]	O0AL[10]	O0AL[9]	O0AL[8]	O0AL[7]	O0AL[6]	O0AL[5]	O0AL[4]	O0AL[3]	O0AL[2]	O0AL[1]	O0AL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	O0AL	0	R/W	OSD Window 0 SDRAM Source Address - Low 16 LSBs of SDRAM source address The SDRAM source address is specified offset from the SDRAM base address in units of32 bytes. **This bit is latched by VD.*

4.12.16 OSDWIN1ADL

OSD Window 1 Address - Low

OSDWIN1ADL 0003:069E offset: 0x1E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O1AL[15]	O1AL[14]	O1AL[13]	O1AL[12]	O1AL[11]	O1AL[10]	O1AL[9]	O1AL[8]	O1AL[7]	O1AL[6]	O1AL[5]	O1AL[4]	O1AL[3]	O1AL[2]	O1AL[1]	O1AL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	O1AL	0	R/W	OSD Window 1 / Attribute Window SDRAM Source Address - Low 16 LSBs of SDRAM source address (specified in 32-byte units) The SDRAM source address is specified offset from the SDRAM base address in units of 32 bytes. **This bit is latched by VD.*

4.12.17 BASEPX

Base Pixel X

BASEPX 0003:06A0 offset: 0x20 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	BPX[9]	BPX[8]	BPX[7]	BPX[6]	BPX[5]	BPX[4]	BPX[3]	BPX[2]	BPX[1]	BPX[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	BPX	0	R/W	Base Pixel in X Horizontal base display reference position for all windows. Specified as number of pixels from HD. Minimum value is 24. **This bit is latched by VD.*

4.12.18 BASEPY

Base Pixel Y

BASEPY 0003:06A2 offset: 0x22 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	BPY[8]	BPY[7]	BPY[6]	BPY[5]	BPY[4]	BPY[3]	BPY[2]	BPY[1]	BPY[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	BPY	0	R/W	Base Pixel(Line) in Y vertical base display reference position for all windows. Specified as number of lines from VD. Value used is MAX(BPY,1), i.e., minumum value is 1. *This bit is latched by VD.*

4.12.19 VIDWIN0XP

Video Window 0 X-Position

VIDWIN0XP 0003:06A4 offset: 0x24 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	V0X[9]	V0X[8]	V0X[7]	V0X[6]	V0X[5]	V0X[4]	V0X[3]	V0X[2]	V0X[1]	V0X[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	V0X	0	R/W	Video Window 0 X-Position Horizontal display start position - number of pixels from display reference position (BASEPX) *This bit is latched by VD.*

4.12.20 VIDWIN0YP

Video Window 0 Y-Position

VIDWIN0YP 0003:06A6 offset: 0x26 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	V0Y[8]	V0Y[7]	V0Y[6]	V0Y[5]	V0Y[4]	V0Y[3]	V0Y[2]	V0Y[1]	V0Y[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	V0Y	0	R/W	Video Window 0 Y-Position Vertical display start position - number of lines from display reference position (BASEPY) **This bit is latched by VD.*

4.12.21 VIDWIN0XL

Video Window 0 X-Size

VIDWIN0XL 0003:06A8 offset: 0x28 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	V0W[11]	V0W[10]	V0W[9]	V0W[8]	V0W[7]	V0W[6]	V0W[5]	V0W[4]	V0W[3]	V0W[2]	V0W[1]	V0W[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	V0W	0	R/W	Video Window 0 X-Width Horizontal display width in pixels *This bit is latched by VD.*

4.12.22 VIDWIN0YL

Video Window 0 Y-Size

VIDWIN0YL 0003:06AA offset: 0x2A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	V0H[10]	V0H[9]	V0H[8]	V0H[7]	V0H[6]	V0H[5]	V0H[4]	V0H[3]	V0H[2]	V0H[1]	V0H[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	V0H	0	R/W	Video Window 0 Y-Height Vertical display height in lines *This bit is latched by VD.*

4.12.23 VIDWIN1XP

Video Window 1 X-Position

VIDWIN1XP 0003:06AC offset: 0x2C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	V1X[9]	V1X[8]	V1X[7]	V1X[6]	V1X[5]	V1X[4]	V1X[3]	V1X[2]	V1X[1]	V1X[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	V1X	0	R/W	Video Window 1 X-Position Horizontal display start position - number of pixels from display reference position (BASEPX) **This bit is latched by VD.*

4.12.24 VIDWIN1YP

Video Window 1 Y-Position

VIDWIN1YP 0003:06AE offset: 0x2E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	V1Y[8]	V1Y[7]	V1Y[6]	V1Y[5]	V1Y[4]	V1Y[3]	V1Y[2]	V1Y[1]	V1Y[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	V1Y	0	R/W	Video Window 1 Y-Position Vertical display start position - number of lines from display reference position (BASEPY) **This bit is latched by VD.*

4.12.25 VIDWIN1XL

Video Window 1 X-Size

VIDWIN1XL 0003:06B0 offset: 0x30 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	V1W[11]	V1W[10]	V1W[9]	V1W[8]	V1W[7]	V1W[6]	V1W[5]	V1W[4]	V1W[3]	V1W[2]	V1W[1]	V1W[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	V1W	0	R/W	Video Window 1 X-Width Horizontal display width in pixels **This bit is latched by VD.*

4.12.26 VIDWIN1YL

Video Window 1 Y-Size

VIDWIN1YL 0003:06B2 offset: 0x32 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	V1H[10]	V1H[9]	V1H[8]	V1H[7]	V1H[6]	V1H[5]	V1H[4]	V1H[3]	V1H[2]	V1H[1]	V1H[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	V1H	0	R/W	Video Window 1 Y-Height Vertical display height in lines **This bit is latched by VD.*

4.12.27 OSDWIN0XP

OSD Bitmap Window 0 X-Position

OSDWIN0XP 0003:06B4 offset: 0x34 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	W0X[9]	W0X[8]	W0X[7]	W0X[6]	W0X[5]	W0X[4]	W0X[3]	W0X[2]	W0X[1]	W0X[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	W0X	0	R/W	OSD Window 0 X-Position Horizontal display start position - number of pixels from display reference position (BASEPX) **This bit is latched by VD.*

4.12.28 OSDWIN0YP

OSD Bitmap Window 0 Y-Position

OSDWIN0YP 0003:06B6 offset: 0x36 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	W0Y[8]	W0Y[7]	W0Y[6]	W0Y[5]	W0Y[4]	W0Y[3]	W0Y[2]	W0Y[1]	W0Y[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	W0Y	0	R/W	OSD Window 0 Y-Position Vertical display start position - number of lines from display reference position (BASEPY) **This bit is latched by VD.*

4.12.29 OSDWIN0XL

OSD Bitmap Window 0 X-Size

OSDWIN0XL 0003:06B8 offset: 0x38 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	W0W[11]	W0W[10]	W0W[9]	W0W[8]	W0W[7]	W0W[6]	W0W[5]	W0W[4]	W0W[3]	W0W[2]	W0W[1]	W0W[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	W0W	0	R/W	OSD Window 0 X-Width Horizontal display width in pixels **This bit is latched by VD.*

4.12.30 OSDWIN0YL

OSD Bitmap Window 0 Y-Size

OSDWIN0YL 0003:06BA offset: 0x3A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	W0H[10]	W0H[9]	W0H[8]	W0H[7]	W0H[6]	W0H[5]	W0H[4]	W0H[3]	W0H[2]	W0H[1]	W0H[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	W0H	0	R/W	OSD Window 0 Y-Height Vertical display height in lines **This bit is latched by VD.*

4.12.31 OSDWIN1XP

OSD Bitmap Window 1 X-Position

OSDWIN1XP 0003:06BC offset: 0x3C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	W1X[9]	W1X[8]	W1X[7]	W1X[6]	W1X[5]	W1X[4]	W1X[3]	W1X[2]	W1X[1]	W1X[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	W1X	0	R/W	OSD Window 1 X-Position Horizontal display start position - number of pixels from display reference position (BASEPX) **This bit is latched by VD.*

4.12.32 OSDWIN1YP

OSD Bitmap Window 1 Y-Position

OSDWIN1YP 0003:06BE offset: 0x3E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	W1Y[8]	W1Y[7]	W1Y[6]	W1Y[5]	W1Y[4]	W1Y[3]	W1Y[2]	W1Y[1]	W1Y[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	W1Y	0	R/W	OSD Window 1 Y-Position Vertical display start position - number of lines from display reference position (BASEPY) **This bit is latched by VD.*

4.12.33 OSDWIN1XL

OSD Bitmap Window 1 X-Size

OSDWIN1XL 0003:06C0 offset: 0x40 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	W1W[11]	W1W[10]	W1W[9]	W1W[8]	W1W[7]	W1W[6]	W1W[5]	W1W[4]	W1W[3]	W1W[2]	W1W[1]	W1W[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	W1W	0	R/W	OSD Window 1 X-Width Horizontal display width in pixels *This bit is latched by VD.*

4.12.34 OSDWIN1YL

OSD Bitmap Window 1 Y-Size

OSDWIN1YL 0003:06C2 offset: 0x42 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	W1H[10]	W1H[9]	W1H[8]	W1H[7]	W1H[6]	W1H[5]	W1H[4]	W1H[3]	W1H[2]	W1H[1]	W1H[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	W1H	0	R/W	OSD Window 1 Y-Height Vertical display height in lines *This bit is latched by VD.*

4.12.35 CURXP

Rectangular Cursor Window X-Position

CURXP 0003:06C4 offset: 0x44 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RCSX[9]	RCSX[8]	RCSX[7]	RCSX[6]	RCSX[5]	RCSX[4]	RCSX[3]	RCSX[2]	RCSX[1]	RCSX[0]
R/W	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9:0	RCSX	0	R/W	Rectangular Cursor Window X-Position Horizontal display start position - number of pixels from display reference position (BASEPX) **This bit is latched by VD.*

4.12.36 CURYP

Rectangular Cursor Window Y-Position

CURYP 0003:06C6 offset: 0x46 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RCSY[8]	RCSY[7]	RCSY[6]	RCSY[5]	RCSY[4]	RCSY[3]	RCSY[2]	RCSY[1]	RCSY[0]
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8:0	RCSY	0	R/W	Rectangular Cursor Window Y-Position Vertical display start position - number of lines from display reference position (BASEPY) **This bit is latched by VD.*

4.12.37 CURXL

Rectangular Cursor Window X-Size

CURXL 0003:06C8 offset: 0x48 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RCSW[11]	RCSW[10]	RCSW[9]	RCSW[8]	RCSW[7]	RCSW[6]	RCSW[5]	RCSW[4]	RCSW[3]	RCSW[2]	RCSW[1]	RCSW[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11:0	RCSW	0	R/W	Rectangular Cursor Window X-Width Horizontal display width in pixels **This bit is latched by VD.*

4.12.38 CURYL

Rectangular Cursor Window Y-Size

CURYL 0003:06CA offset: 0x4A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RCSH[10]	RCSH[9]	RCSH[8]	RCSH[7]	RCSH[6]	RCSH[5]	RCSH[4]	RCSH[3]	RCSH[2]	RCSH[1]	RCSH[0]
R/W	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
10:0	RCSH	0	R/W	Rectangular Cursor Window Y-Height Vertical display height in lines **This bit is latched by VD.*

4.12.39 W0BMP01

Window 0 Bitmap Value to Palette Map 0/1

W0BMP01 0003:06D0 offset: 0x50 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL01[7]	PAL01[6]	PAL01[5]	PAL01[4]	PAL01[3]	PAL01[2]	PAL01[1]	PAL01[0]	PAL00[7]	PAL00[6]	PAL00[5]	PAL00[4]	PAL00[3]	PAL00[2]	PAL00[1]	PAL00[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL01	0	R/W	Palatte Address for Bitmap Value 1 - OSD Window 0 [4-bit]
7:0	PAL00	0	R/W	Palatte Address for Bitmap Value 0 - OSD Window 0 [4-bit, 2-bit, 1-bit]

4.12.40 W0BMP23

Window 0 Bitmap Value to Palette Map 2/3

W0BMP23 0003:06D2 offset: 0x52 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL03[7]	PAL03[6]	PAL03[5]	PAL03[4]	PAL03[3]	PAL03[2]	PAL03[1]	PAL03[0]	PAL02[7]	PAL02[6]	PAL02[5]	PAL02[4]	PAL02[3]	PAL02[2]	PAL02[1]	PAL02[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL03	0	R/W	Palatte Address for Bitmap Value 3 - OSD Window 0 [4-bit]
7:0	PAL02	0	R/W	Palatte Address for Bitmap Value 2 - OSD Window 0 [4-bit]

4.12.41 W0BMP45

Window 0 Bitmap Value to Palette Map 4/5

W0BMP45 0003:06D4 offset: 0x54 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL05[7]	PAL05[6]	PAL05[5]	PAL05[4]	PAL05[3]	PAL05[2]	PAL05[1]	PAL05[0]	PAL04[7]	PAL04[6]	PAL04[5]	PAL04[4]	PAL04[3]	PAL04[2]	PAL04[1]	PAL04[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL05	0	R/W	Palatte Address for Bitmap Value 5 - OSD Window 0 [4-bit, 2-bit]
7:0	PAL04	0	R/W	Palatte Address for Bitmap Value 4 - OSD Window 0 [4-bit]

4.12.42 W0BMP67

Window 0 Bitmap Value to Palette Map 6/7

W0BMP67 0003:06D6 offset: 0x56 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL07[7]	PAL07[6]	PAL07[5]	PAL07[4]	PAL07[3]	PAL07[2]	PAL07[1]	PAL07[0]	PAL06[7]	PAL06[6]	PAL06[5]	PAL06[4]	PAL06[3]	PAL06[2]	PAL06[1]	PAL06[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL07	0	R/W	Palatte Address for Bitmap Value 7 - OSD Window 0 [4-bit]
7:0	PAL06	0	R/W	Palatte Address for Bitmap Value 6 - OSD Window 0 [4-bit]

4.12.43 W0BMP89

Window 0 Bitmap Value to Palette Map 8/9

W0BMP89 0003:06D8 offset: 0x58 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL09[7]	PAL09[6]	PAL09[5]	PAL09[4]	PAL09[3]	PAL09[2]	PAL09[1]	PAL09[0]	PAL08[7]	PAL08[6]	PAL08[5]	PAL08[4]	PAL08[3]	PAL08[2]	PAL08[1]	PAL08[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL09	0	R/W	Palatte Address for Bitmap Value 9 - OSD Window 0 [4-bit]
7:0	PAL08	0	R/W	Palatte Address for Bitmap Value 8 - OSD Window 0 [4-bit]

4.12.44 W0BMPAB

Window 0 Bitmap Value to Palette Map A/B

W0BMPAB 0003:06DA offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL11[7]	PAL11[6]	PAL11[5]	PAL11[4]	PAL11[3]	PAL11[2]	PAL11[1]	PAL11[0]	PAL10[7]	PAL10[6]	PAL10[5]	PAL10[4]	PAL10[3]	PAL10[2]	PAL10[1]	PAL10[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL11	0	R/W	Palatte Address for Bitmap Value B - OSD Window 0 [4-bit]
7:0	PAL10	0	R/W	Palatte Address for Bitmap Value A - OSD Window 0 [4-bit, 2-bit]

4.12.45 W0BMPCD

Window 0 Bitmap Value to Palette Map C/D

W0BMPCD 0003:06DC offset: 0x5C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL13[7]	PAL13[6]	PAL13[5]	PAL13[4]	PAL13[3]	PAL13[2]	PAL13[1]	PAL13[0]	PAL12[7]	PAL12[6]	PAL12[5]	PAL12[4]	PAL12[3]	PAL12[2]	PAL12[1]	PAL12[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL13	0	R/W	Palatte Address for Bitmap Value D - OSD Window 0 [4-bit]
7:0	PAL12	0	R/W	Palatte Address for Bitmap Value C - OSD Window 0 [4-bit]

4.12.46 W0BMPEF

Window 0 Bitmap Value to Palette Map E/F

W0BMPEF 0003:06DE offset: 0x5E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL15[7]	PAL15[6]	PAL15[5]	PAL15[4]	PAL15[3]	PAL15[2]	PAL15[1]	PAL15[0]	PAL14[7]	PAL14[6]	PAL14[5]	PAL14[4]	PAL14[3]	PAL14[2]	PAL14[1]	PAL14[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL15	0	R/W	Palatte Address for Bitmap Value F - OSD Window 0 [4-bit, 2-bit, 1-bit]
7:0	PAL14	0	R/W	Palatte Address for Bitmap Value E - OSD Window 0 [4-bit]

4.12.47 W1BMP01

Window 1 Bitmap Value to Palette Map 0/1

W1BMP01 0003:06E0 offset: 0x60 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL01[7]	PAL01[6]	PAL01[5]	PAL01[4]	PAL01[3]	PAL01[2]	PAL01[1]	PAL01[0]	PAL00[7]	PAL00[6]	PAL00[5]	PAL00[4]	PAL00[3]	PAL00[2]	PAL00[1]	PAL00[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL01	0	R/W	Palatte Address for Bitmap Value 1 - OSD Window 1 [4-bit]
7:0	PAL00	0	R/W	Palatte Address for Bitmap Value 0 - OSD Window 1 [4-bit, 2-bit, 1-bit]

4.12.48 W1BMP23

Window 1 Bitmap Value to Palette Map 2/3

W1BMP23 0003:06E2 offset: 0x62 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL03[7]	PAL03[6]	PAL03[5]	PAL03[4]	PAL03[3]	PAL03[2]	PAL03[1]	PAL03[0]	PAL02[7]	PAL02[6]	PAL02[5]	PAL02[4]	PAL02[3]	PAL02[2]	PAL02[1]	PAL02[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL03	0	R/W	Palatte Address for Bitmap Value 3 - OSD Window 1 [4-bit]
7:0	PAL02	0	R/W	Palatte Address for Bitmap Value 2 - OSD Window 1 [4-bit]

4.12.49 W1BMP45

Window 1 Bitmap Value to Palette Map 4/5

W1BMP45 0003:06E4 offset: 0x64 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL05[7]	PAL05[6]	PAL05[5]	PAL05[4]	PAL05[3]	PAL05[2]	PAL05[1]	PAL05[0]	PAL04[7]	PAL04[6]	PAL04[5]	PAL04[4]	PAL04[3]	PAL04[2]	PAL04[1]	PAL04[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL05	0	R/W	Palatte Address for Bitmap Value 5 - OSD Window 1 [4-bit, 2-bit]
7:0	PAL04	0	R/W	Palatte Address for Bitmap Value 4 - OSD Window 1 [4-bit]

4.12.50 W1BMP67

Window 1 Bitmap Value to Palette Map 6/7

W1BMP67 0003:06E6 offset: 0x66 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL07[7]	PAL07[6]	PAL07[5]	PAL07[4]	PAL07[3]	PAL07[2]	PAL07[1]	PAL07[0]	PAL06[7]	PAL06[6]	PAL06[5]	PAL06[4]	PAL06[3]	PAL06[2]	PAL06[1]	PAL06[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL07	0	R/W	Palatte Address for Bitmap Value 7 - OSD Window 1 [4-bit]
7:0	PAL06	0	R/W	Palatte Address for Bitmap Value 6 - OSD Window 1 [4-bit]

4.12.51 W1BMP89

Window 1 Bitmap Value to Palette Map 8/9

W1BMP89 0003:06E8 offset: 0x68 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL09[7]	PAL09[6]	PAL09[5]	PAL09[4]	PAL09[3]	PAL09[2]	PAL09[1]	PAL09[0]	PAL08[7]	PAL08[6]	PAL08[5]	PAL08[4]	PAL08[3]	PAL08[2]	PAL08[1]	PAL08[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL09	0	R/W	Palatte Address for Bitmap Value 9 - OSD Window 1 [4-bit]
7:0	PAL08	0	R/W	Palatte Address for Bitmap Value 8 - OSD Window 1 [4-bit]

4.12.52 W1BMPAB

Window 1 Bitmap Value to Palette Map A/B

W1BMPAB 0003:06EA offset: 0x6A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL11[7]	PAL11[6]	PAL11[5]	PAL11[4]	PAL11[3]	PAL11[2]	PAL11[1]	PAL11[0]	PAL10[7]	PAL10[6]	PAL10[5]	PAL10[4]	PAL10[3]	PAL10[2]	PAL10[1]	PAL10[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL11	0	R/W	Palatte Address for Bitmap Value B - OSD Window 1 [4-bit]
7:0	PAL10	0	R/W	Palatte Address for Bitmap Value A - OSD Window 1 [4-bit, 2-bit]

4.12.53 W1BMPCD

Window 1 Bitmap Value to Palette Map C/D

W1BMPCD 0003:06EC offset: 0x6C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL13[7]	PAL13[6]	PAL13[5]	PAL13[4]	PAL13[3]	PAL13[2]	PAL13[1]	PAL13[0]	PAL12[7]	PAL12[6]	PAL12[5]	PAL12[4]	PAL12[3]	PAL12[2]	PAL12[1]	PAL12[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL13	0	R/W	Palatte Address for Bitmap Value D - OSD Window 1 [4-bit]
7:0	PAL12	0	R/W	Palatte Address for Bitmap Value C - OSD Window 1 [4-bit]

4.12.54 W1BMPEF

Window 1 Bitmap Value to Palette Map E/F

W1BMPEF 0003:06EE offset: 0x6E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAL15[7]	PAL15[6]	PAL15[5]	PAL15[4]	PAL15[3]	PAL15[2]	PAL15[1]	PAL15[0]	PAL14[7]	PAL14[6]	PAL14[5]	PAL14[4]	PAL14[3]	PAL14[2]	PAL14[1]	PAL14[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	PAL15	0	R/W	Palatte Address for Bitmap Value F - OSD Window 1 [4-bit, 2-bit, 1-bit]
7:0	PAL14	0	R/W	Palatte Address for Bitmap Value E - OSD Window 1 [4-bit]

4.12.55 MISCCTL

Miscellaneous Control

MISCCTL 0003:06F4 offset: 0x74 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	CPBSY	PPSW	PPRV	RSV
R/W	-	-	-	-	-	-	-	-	-	-	-	-	R	R/W	R/W	-
Default	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-

Bit	Name	Reset Value	R/W	Function
15:4	RSV			Reserved
3	CPBSY	0	R	CLUT Write Busy Used when writing CLUT data to RAM. » 0: Not busy, okay to write « » 1: Busy, do not write «
2	PPSW	0	R/W	Ping-pong buffer toggle select When PPRV=0: 0: Use SDRAM address in VIDWINADH / VIDWIN0ADL 1: Use SDRAM address in PPVWINAD0H / PPVWIN0ADL When PPRV=1 0: Use SDRAM address in PPVIDWIN0H / PPVIDWIN0L 1: Use SDRAM address in VIDWINADH / VIDWIN0ADL
1	PPRV	0	R/W	Ping-pong buffer Reverse Inverts polarity of internal select signal. Affects bit PPSW.
0	RSV	0	R/W	Reserved, please set to 0.

4.12.56 CLUTRAMYCB

CLUT RAM Y/Cb Setup

CLUTRAMYCB 0003:06F6 offset: 0x76 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	CB[7]	CB[6]	CB[5]	CB[4]	CB[3]	CB[2]	CB[1]	CB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	Y	0	R/W	Write Y-data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR
7:0	CB	0	R/W	Write Cb-data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR

4.12.57 CLUTRAMCR

CLUT RAM Cr/Mapping Setup

CLUTRAMCR 0003:06F8 offset: 0x78 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CR[7]	CR[6]	CR[5]	CR[4]	CR[3]	CR[2]	CR[1]	CR[0]	CADDR[7]	CADDR[6]	CADDR[5]	CADDR[4]	CADDR[3]	CADDR[2]	CADDR[1]	CADDR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	CR	0	R/W	Write Cr data into built-in CLUT-RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR
7:0	CADDR	0	R/W	CLUT Write Palette Address When updating CLUT-RAM: - verify CPBSY=0 in MISCCTL and - write CLUTRAMYCB before CLUTRAMCR.

4.12.58 PPVWIN0ADH

Ping-Pong Video Window 0 Address (High)

PPVWIN0ADH 0003:06FC offset: 0x7C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	V0PAH[6]	V0PAH[5]	V0PAH[4]	V0PAH[3]	V0PAH[2]	V0PAH[1]	V0PAH[0]
R/W	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:7	RSV			Reserved
6:0	V0PAH	0	R/W	Ping-pong Video Window 0 Address (High) 7 MSBs of SDRAM source address (specified in 32-byte units) **This bit is latched by VD.*

4.12.59 PPVWIN0ADL

Ping-Pong Video Window 0 Address (Low)

PPVWIN0ADL 0003:06FE offset: 0x7E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	V0PAL[15]	V0PAL[14]	V0PAL[13]	V0PAL[12]	V0PAL[11]	V0PAL[10]	V0PAL[9]	V0PAL[8]	V0PAL[7]	V0PAL[6]	V0PAL[5]	V0PAL[4]	V0PAL[3]	V0PAL[2]	V0PAL[1]	V0PAL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Reset Value	R/W	Function
15:0	V0PAL	0	R/W	Ping-pong Video Window 0 Address (Low) 16 LSBs of SDRAM source address (specified in 32-byte units) **This bit is latched by VD.*

5 Video Encoder

5.1 Introduction

The Video Encoder is used to display images and video on TV monitor and various LCD displays. The Video Encoder converts digital YCbCr signals to analog and digital video signals. The Video Encoder can generate composite NTSC or PAL signals, and 8-bit digital LCD interface signals. To generate these signals, the Video Encoder has digital to analog converter, a digital LCD interface, and a set of signals to perform timing and synchronization. The block diagram for Video Encoder is shown in the ***Error! Reference source not found.***.

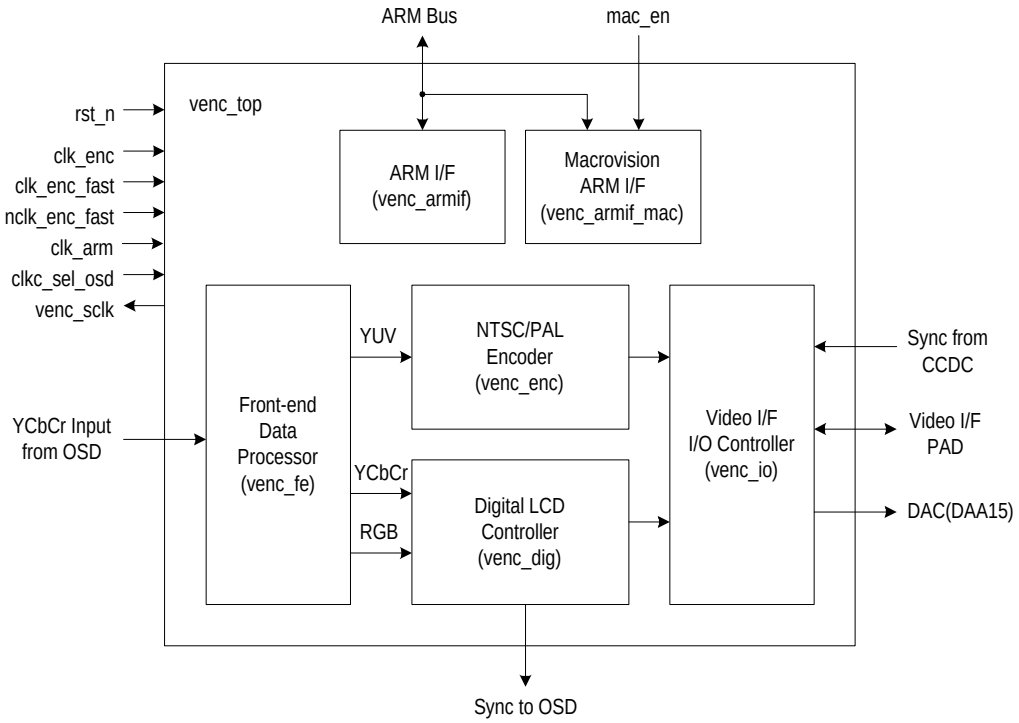


Figure 1: Video Encoder Block Diagram

5.1.1 Composite Analog Video Encoder features (NTSC/PAL)

- Master Clock Input - 27MHz
- 10-bit D/A Output Interface with output control
- NTSC/PAL Output Selectable
- Video Attribute Insertion (NTSC – Line 20, PAL – Line 23)
- Interlace/Non-Interlace selected output
- Setup Selection for NTSC
- VSYNC/ HSYNC Output
- Selectable VSYNC/Composite SYNC Output
- 16-235/0-255 Input Amplitude Selectable
- Video Output Blanking
- Chrominance Low Pass Filter 1.5MHz/3MHz
- Internal Color Bar Generation (100/75%)
- Closed caption support

5.1.2 Digital RGB/YUV Interface features

- Programmable DCLK out for Digital-RGB Output
- Supports various output formats
  - YCbCr 16 bit
  - YcbCr 8 bit
  - ITU-R BT.656
  - RGB 18-bit
  - RGB 8-bit
  - DisplayTech QVGA
  - STN
- Digital Low Pass Filter for RGB Output
- Digital VSYNC/HSYNC output
- Programmable Timing generators
- Built-in timing generators for EPSON/CASIO LCD panels
- Master-slave operation
- Internal Color Bar Generation (100/75%)

5.2 Video Encoder Operating Modes

5.2.1 Video Mode

The DM320 VENC supports the video modes discussed in following sections.

5.2.1.1 NTSC/PAL standard mode

DM320 VENC operates as the NTSC/PAL encoder. 525/60(NTSC) or 625/50 (PAL) formats are supported. For NTSC/PAL CVBS output, the VENC should be operated in this mode. The digital output for the LCD is also available simultaneously. The NTPLS field of VMOD register selects NTSC/PAL formats.

5.2.1.2 Nonstandard mode

This is a dedicated mode for digital LCD. In this mode the VENC operates at any given timing by register setting. To select non-standard mode, set 1 to the VMD field of register VMOD.

5.2.2 Synchronous Mode

The DM320 VENC supports two synchronous modes: master and slave. This can be used in above two video modes.

5.2.2.1 Master mode

This operates in synchronization with horizontal / vertical sync signals generated in built-in sync signal generator.

5.2.2.2 Slave mode

This operates in synchronization with sync signals input from outside. Set SLAVE bit of VMOD register to '1' when slave mode is used. When EXSYNC bit of SYNCTL register is '0', the external inputs from the HSYNC/VSYNC pins are used as external sync signals. When EXSYNC = '1', the sync signals from the CCDC are used as external sync signals. This provides synchronizing the CCD timing and the video output timing. The polarity of external sync input is active high by default. It is possible to invert by EXHIV, EXVIV of SYNCTL. The field ID can be applied in the following combination. The external field input mode is enabled by setting EXFEN bit in SYNCTL register.

EXFEN	EXSYNC	Field ID Mode
0	-	Use field ID generated internally
1	0	Field ID is fixed to '0'
	1	Use field ID generated in the CCDC.

5.3 Front-end Data Processing

The front-end data processor receives the YCbCr pixel data from the OSD module and converts it into the digital YCbCr, YUV and RGB representation.

Figure 55shows the block diagram of the front-end data processor. The 8 bit YCbCr pixel data from the OSD passes through the low-pass filter (pre-filter) at the very beginning of the data path. Then it is multiplexed with the internal color bar. The level attenuator has a role to compress the signal level with 0-255 into the ITU-R BT.601 specified level (Y:16-235, C:16-240). Each data path (digital YCbCr, digital RGB and YUV) has its own attenuator. After attenuation, for TV encoder path, the appropriate gain is applied to the attenuated Y, Cb and Cr. For the digital RGB data path, the RGB conversion matrix is applied. For the digital YCbCr, the attenuated YCbCr is used. Each data path is properly adjusted for the delay timing to match the output latency.

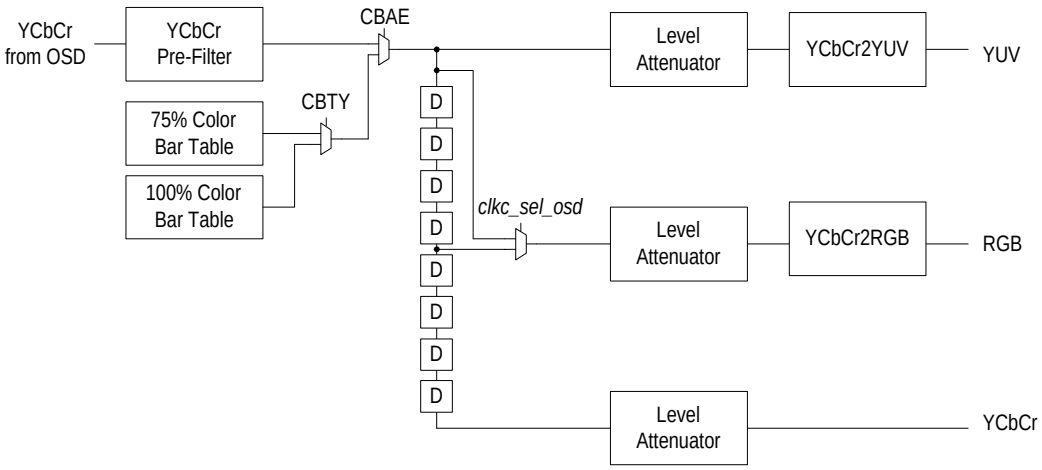


Figure 55: Front-end Data Processor Block Diagram

5.3.1 YCbCr Pre-filter

The pre-filter structure resides at the beginning of the data path. Each component (Y, Cb and Cr) has its own filter. The filter length can be programmed to 2 or 3 tap by PFLTY bit for Y and PFLTC bit for C in the VDPRO register. The sampling rate can be chosen as CLK_ENC or CLK_ENC/2 by PFLTR bit of VDPRO register.

5.3.2 Level Attenuator

The VENC assumes the two possibilities for the level of the input video data. One is the data conforming to the ITU-RBT.601 specified level, namely Y is ranged between 16-235 and C is between 16-240. Another is the data with the range of 0-255 for Y, C. The attenuator compresses the data with the range of 0-255 into the ITU-R BT.601 specified level. User can independently choose whether or not to apply the attenuation by bits ATCMP, ATYCC and ATRGB of VDPRO register for each data path.

5.3.3 YUV Conversion

The proper gain is applied to attenuated YCbCr data and then it is converted into YUV signals for CVBS generation. When STUP bit of VDPRO register is ‘1’, 7.5% setup offset is added for the output. The STUP is effective both for NTSC or PAL. However for PAL mode setting STUP to 1 causes illegal output level. The gains are different in each component and each video mode (NTSC, NTSC with setup or PAL).

The BLNK bit of VMOD register is the blanking enable. When this is set to 1, CVBS output is blanked without regard to input video signals. There is a multiplexer for replacing the input data by blanking level in ITU-R BT.601.

5.3.4 RGB Conversion

VENC supports YCbCr to RGB conversion. The conversion matrixes are selectable by the RGBMAT bit of VDPRO register. Since the converted RGB may become negative due to finite precision arithmetic operation, zero level clipping is applied. The offset specified by OFST field of RGBCLP register is added followed by the upper level clipping. The level for clipping is set by UCLIP field of RGBCLP register. The output RGB is 8 bits in length.

5.4 NTSC/PAL Video Encoder

Figure 56shows the block diagram of the NTSC/PAL video encoder block. The NTSC/PAL encoder supports PAL-M/N on trial in addition to NTSC and general PAL.

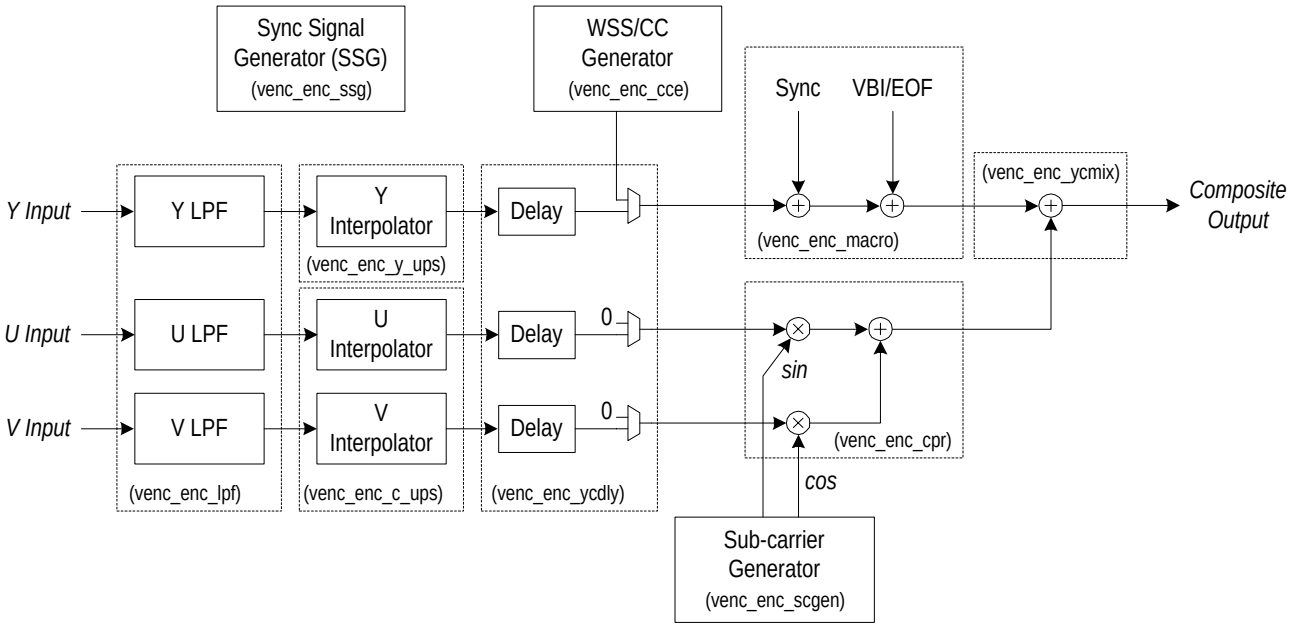


Figure 56 NTSC/PAL Encoder block diagram

5.4.1 Luma Signal Processing

The Y signal from the front end data processor is applied to x2 interpolation after an optional low-pass filter. The interpolation filter is 11 taps filter. The interpolation is disabled by default and can be enabled by setting bit YUPS of VDPRO register. When the OSD is in same clock mode, the interpolation is disabled by force since pixel rate is already 27MHz.

5.4.2 Chroma Signal Processing

The chroma signal is also applied to the x2 interpolation. The interpolation filter is 7 tap filter. The chroma upsampling is disabled by default and can be enabled by bit CUPS in VDPRO register.

5.4.3 CVBS Generation

The upsampled Y signal and upsampled chroma signals (U and V) after the luma and chroma signal processing modules , are mixed together in the YC mixer the mixed signal is output to the DAC. Setting bit VIE in VMOD register to 0 can force DAC input to L level regardless the output of YC mixer.

5.4.4 Y/C Delay

The delays on Y and C signals are aligned at those signals are mixed at the YC mixer module. The bit YCDLY of VDPRO register can adjust the delay of the Y component within –4 to 3 ENC clock.

5.4.5 Sub-carrier Generation

The video encoder generates the sub-carrier by internal DDS (Direct Digital Synthesizer). The phase resolution of DDS is (1/1024)*360°. SC-H (Sub-carrier to Horizontal) phase can be controlled by user. First the initial phase value (0 to 1023) has to be written to the field SCSD of SCPROG register and then bit SCPRG of VDPRO register has to set to 1. Writing 1 to this bit automatically updates the sub-carrier phase. Update is occurred at the line 9 in the color field 1 for both NTSC and PAL. Writing 0 put back to the preset phase in same manner when writing 1. By default, preset value by which SC-H phase will close to 0° is applied.

Mode	Preset Value
NTSC	60
PAL	375
PAL-M	375
PAL-N	375

Figure 57 Sub-carrier Initial Phase Default Value

The frequency of sub-carrier is calculated by 3 parameters that are SRATE, SCCP and SCCN as follows,

$$f_{sc} = \frac{1}{1024} \times \left(SRATE - \frac{SCCN}{SCCP - SCCN} \right) \times 27MHz$$

The default number of these parameters are defined as in Figure 58.

Mode	SRATE	SCCN	SCCP
NTSC	135	-25	33-25
PAL	168	-2516	16875-2516
PAL-M	135	-87	143-87
PAL-N	135	-14391	16875-14391

Figure 58 Sub-carrier Parameter Default Value

5.4.6 Video Attribute Insertion

The video encoder has capability to insert video information into the vertical blanking period. For example, the video encoder can insert a video attribute which indicates the proper aspect ratio to the video receiver.

For NTSC mode, the video encoder can insert 14-bit video information on line 20 of every field to conform to the EIAJ CPX-1024 Video Aspect Ratio ID specification. Attribute information should be set using the ATR1and ATR0 registers. The ATR2register should be set with the 6-bit CRC data. Bit7 of the ATR2register enables attribute insertion.

For PAL mode, the video encoder can insert 14-bit video information (WSS) on line 20 of every frame to conform to the ETS 300-294 Wide Screen Signaling specification. Attribute information should be set in the ATR1register and bits5:0 of the ATR2register. Bit 7 of the ATR2register enables attribute insertion.

In NTSC and PAL encoding modes, data in the ATR1 and ATR0registers are transferred to internal circuitry when the ATR2register is set. For this reason, the ATR2register should be set last.

5.4.7 Closed Caption

The DM320 VENC supports closed caption encoding (DSC former devices did not support). Closed caption data is transmitted on the line 21 of the odd field and the line 284 of the even field. It is possible to specify the fields on which closed captioning is enabled by CAPF of CAPCTL register. The data should be written to CAPDO or CAPDE registers for odd or even field respectively. It is required to load the data at least 1 line before. When data is written to CAPDO or CAPDE , the bit CAOST or CAEST of VSTAT register is changed to 1. This bit is automatically cleared to 0 when a caption data transmission is completed on the line 21 in odd field or the line 284 in even field. When the caption data registers CAPDO or CAPDE are not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by CADF of CAPCTL register is automatically transmitted for closed caption data. The width of every data register is 7bit and the parity bit is automatically calculated by hardware.

5.4.8 Horizontal Timing

The timing such as location of horizontal sync pulses, color burst position and active video position is automatically calculated by hardware. Figure 59 and Figure 60 show horizontal timing characteristics for NTSC and PAL respectively. Figure 61 shows the parameter of the timing chart. Note that every duration between steps is two ENC clocks.

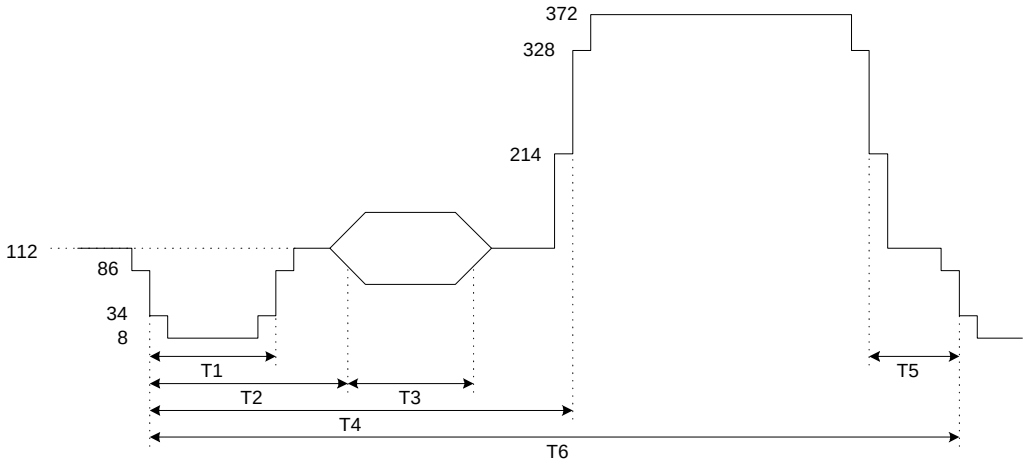


Figure 59 NTSC Horizontal Timing

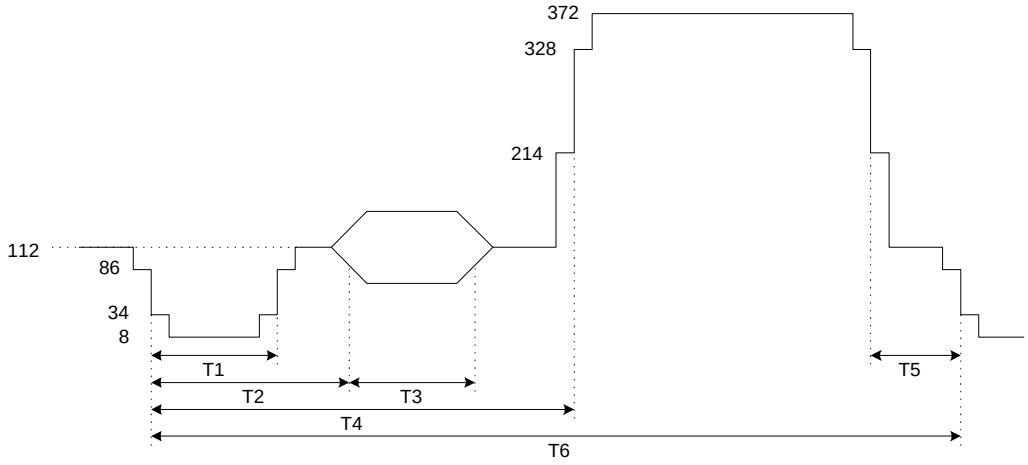


Figure 60 PAL Horizontal Timing

Parameter	Item	NTSC	PAL
T1	Horizontal Sync Pulse Width	126	128
T2	H Ref to Burst Start	147	155
T3	Burst	67	61
T4	H ref to H Blanking End	257	276
T5	Front porch	41	46
T6	1H	1716	1728

Figure 61 Horizontal Timing Parameters

5.4.9 Vertical Timing

The vertical timing is also controlled by hardware automatically for each mode (NTSC or PAL). Serration and equalization pulses are generated for appropriate lines. Color burst is automatically disabled on appropriate lines.

Figure 62 and Figure 63 shows the vertical timing characteristics for each NTSC and PAL modes. The signals appeared in these figures are generated in SSG (sync signal generator) block in the module.

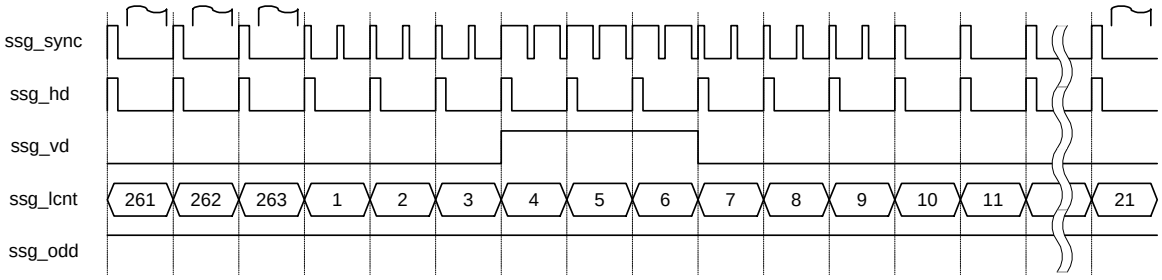


Figure 62 Non-Interlace NTSC Vertical Timing

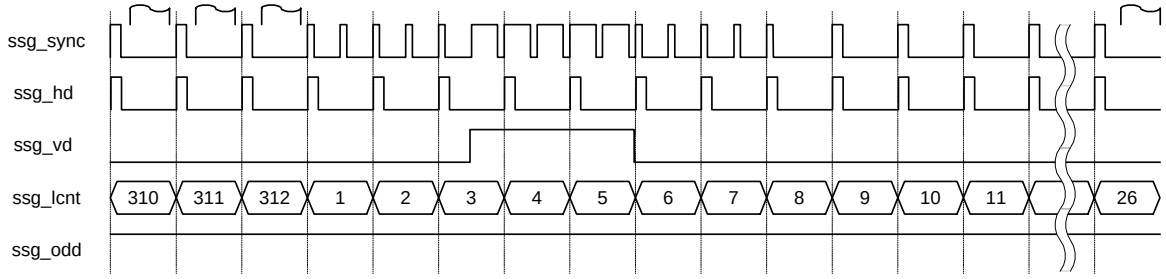


Figure 63 Non-Interlace PAL Vertical Timing

5.4.10 Internal Color Bar

The NTSC/PAL encoder can internally generate color bar by itself. Setting 1 to the CBAE bit of VMOD register enables internal color bar generator. The CBTY bit of VMOD register switches the saturation of the color bar.Set 0 for 75%, 1 for 100%.

5.5 Digital LCD Controller

Figure 64 shows the block diagram of the digital LCD controller block.

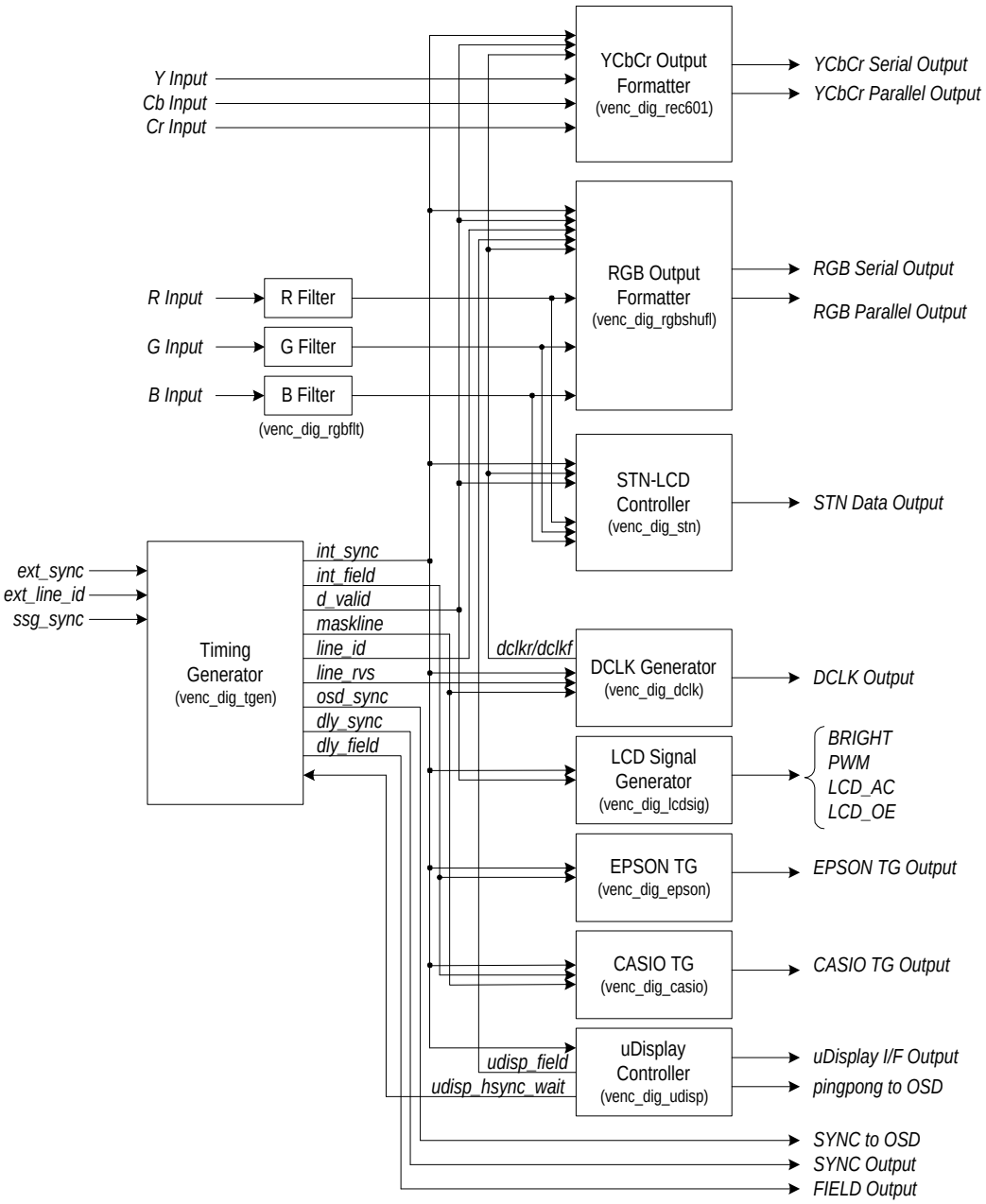


Figure 64 Digital LCD Controller Block Diagram

5.5.1 Digital Video Output Mode

DM320 video encoder supports 8 digital output modes. The mode can be selected by VDMD filed of VMOD register. Figure 65 describes the various modes of the video encoder. The output pins of video encoder acts differently in different video modes as shown in Figure 66.

VDMD	Mode	Description
0	YCC16	To output 16-bit YCbCr(4:2:2) in ITU-R BT.601 format.
1	YCC8	To output 8-bit YCbCr(4:2:2). This supports ITU-R BT.656 output.
2	RGB666	To output 18-bit RGB(6:6:6).
3	RGB8	To output signals for standard LCD.
4	EPSON	To output signals for LCD manufactured by EPSON.
5	CASIO	To output signals for LCD manufactured by CASIO.
6	UDISP	For DisplayTech QVGA (uDisplay)
7	STN	STN-LCD

Figure 65 Digital Video Output Mode

Pin Name	YCC16	YCC8	RGB666	RGB8	EPSON	CASIO	UDISP	STN
YOUT7	Y7	Data7	R7	Data7	Data5	Data5	Data7	Data7
YOUT6	Y6	Data6	R6	Data6	Data4	Data4	Data6	Data6
YOUT5	Y5	Data5	R5	Data5	Data3	Data3	Data5	Data5
YOUT4	Y4	Data4	R4	Data4	Data2	Data2	Data4	Data4
YOUT3	Y3	Data3	R3	Data3	Data1	Data1	Data3	Data3
YOUT2	Y2	Data2	G7	Data2	Data0	Data0	Data2	Data2
YOUT1	Y1	Data1	G6	Data1	GCP	STBYB	Data1	Data1
YOUT0	Y0	Data0	G5	Data0	LP	RIT	Data0	Data0
COUT7	C7	LCD_AC	G4	LCD_AC	RES	CP	LCD_AC	LCD_AC
COUT6	C6	LCD_OE	G3	LCD_OE	XINH	STH	DVALID	LCD_OE
COUT5	C5	BRIGHT	G2	BRIGHT	YSCL	STB	BRIGHT	BRIGHT
COUT4	C4	PWM	B7	PWM	YSCLD	GPCK	PWM	PWM
COUT3	C3	CSYNC	B6	CSYNC	FRYS	GRES	UDISP_FS	Data11
COUT2	C2	0	B5	0	FRYP	POL	0	Data10
COUT1	C1	0	B4	0	FRX	0	BALANCE	Data9
COUT0	C0	0	B3	0	DY	GSRT	FULL	Data8
GIO34	N/A	N/A	R2	N/A	N/A	N/A	N/A	N/A
GIO38	N/A	N/A	B2	EXTLINE_ID	N/A	N/A	N/A	N/A
GIO39	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD	LCD_OE/FIELD

Figure 66 Output Signals in Each Video Output Mode

5.5.2 Timing Generator

The digital LCD controller provides a programmable timing generator. User can generate any non-standard timing other than NTSC/PAL format and use it as basic timing for LCD control. Figure 67 shows the block diagram of the timing generator.

Non-Std Sync Generator creates non-standard horizontal and vertical sync signals as specified in HINT and VINT registers. For NTSC/PAL standard timing, SSG(sync signal generator) can create the timing signals. SSG is a sub-module in the NTSC/PAL encoder block. The sync signals from non-standard and

standard sync generators are multiplexed then used as the fundamental sync signal.

In addition, rising edge detected pulse and counter signals are also generated as the fundamental timing signal. Only these signals manage all timing in the digital LCD controller. Sync generator also produces OSD sync signals. The OSD sync signals are advanced of 8 pixel clock in order to cancel the data path delay which occurs in the front-end data processing. The OSD sync signals are active low while any others are active high signals because the OSD module requires active low signals.

"Valid Generator" generates the data valid signal that is the basis of the LCD_OE output. The assertion timing can be configured by HSTART, VSTART registers and valid duration can be programmed by HVALID, VVALID registers.

"Sync Pulse Generator" takes a role to produce sync signal output to chip outside. HSPLS and VSPLS registers program the pulse width of the output sync signals. User can delay the output sync signals by HSDLY and VSDLY registers without affecting the timing of the internal sync signals. The standard sync signals can also be delayed by these registers.

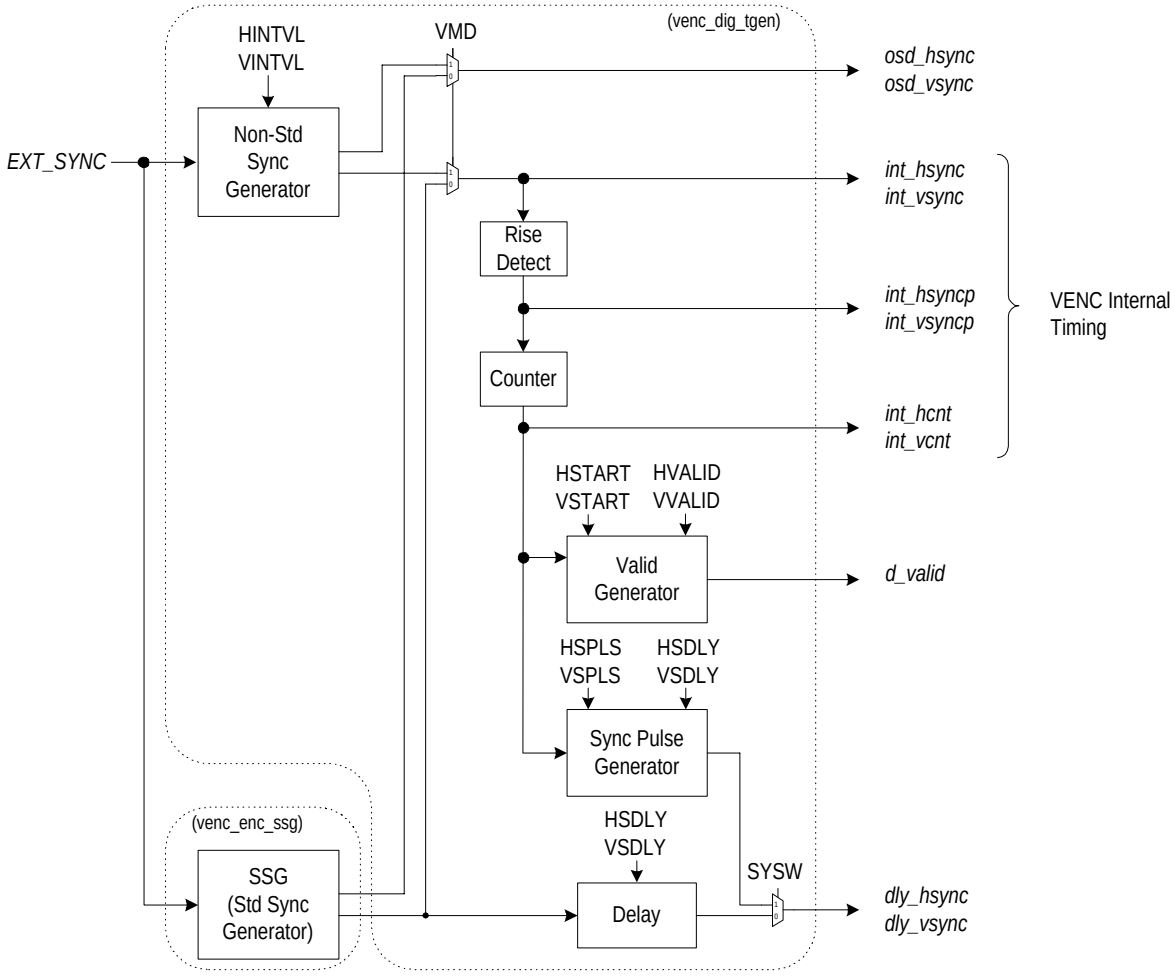


Figure 67 Timing Generator Functional Diagram

Figure 68 shows the timing diagram of basic timing signals generated by timing generator (HSYNC, VSYNC and LCD_OE). In standard mode operation, horizontal and vertical intervals are fixed to NTSC/PAL timing.

Figure 68 shows the basic timing signals diagram and Figure 69 lists the timing generator related registers.

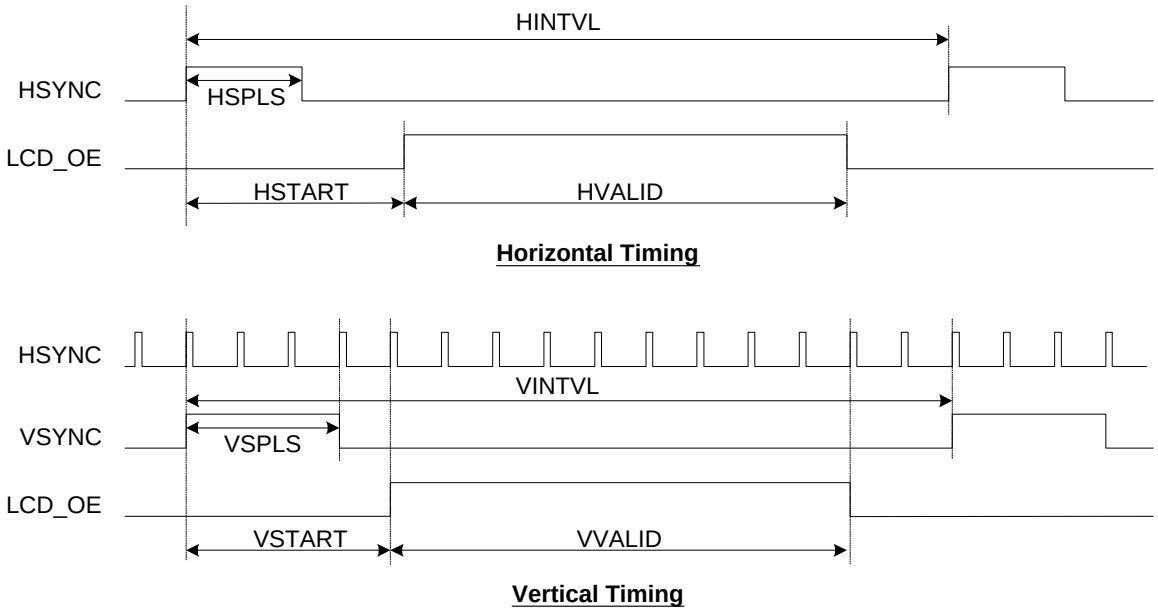


Figure 68 Timing Diagram of Basic Timing Signals

Register	Offset	Description	Unit
HSPLS[12-0]	0x04	HSYNC pulse width.	clk_enc
VSPLS[12-0]	0x05	VSYNC pulse width.	line
HINTVL[12-0]	0x06	HSYNC interval.	clk_enc
HSTART[12-0]	0x07	Horizontal data valid start position.	clk_enc
HVALID[12-0]	0x08	Horizontal data valid duration.	clk_enc
VINTVL[12-0]	0x09	VSYNC interval.	line
VSTART[12-0]	0x0A	Vertical data valid start position.	line
VVALID[12-0]	0x0B	Vertical data valid duration.	line
HSDLY[12-0]	0x0C	HSYNC delay.	clk_enc
VSDLY[12-0]	0x0D	VSYNC delay.	clk_enc

Figure 69 Timing Generator Related Registers

5.5.3 DCLK Generator

The LCD controller can generate dot clock called DCLK that is fed to LCD panels. The generated DCLK is output from VCLK pin. Frequency, waveform and valid duration of the DCLK can be programmed by register settings with various options. The digital data is output in synchronization to the rising edge of DCLK.

5.5.3.1 Pattern Register

The DCLKPTN register is provided for DCLK waveform configuration. User can configure various waveform for DCLK up to within 64 cycles period. The register is 64bit length mapped onto four 16bit registers (DCLKPTN0-DCLKPTN3). The effective pattern length can be specified in DCKPW of DCLKCTL register. Moreover, another pattern register with same structure (DCLKPTN0A-DCLKPTN3A)is optionally provided. This enables user to switch the waveform by every certain line. Figure 70 shows DCLK pattern register configuration scheme.

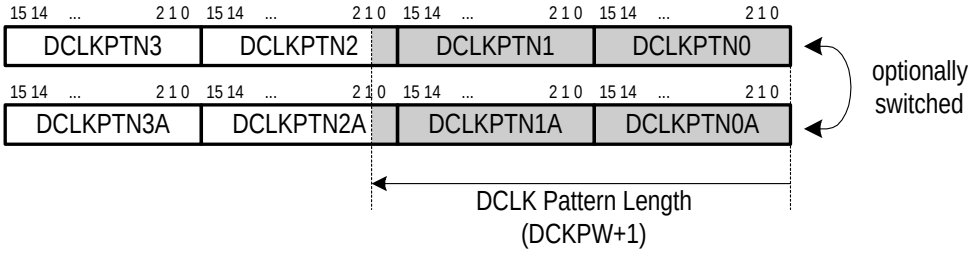
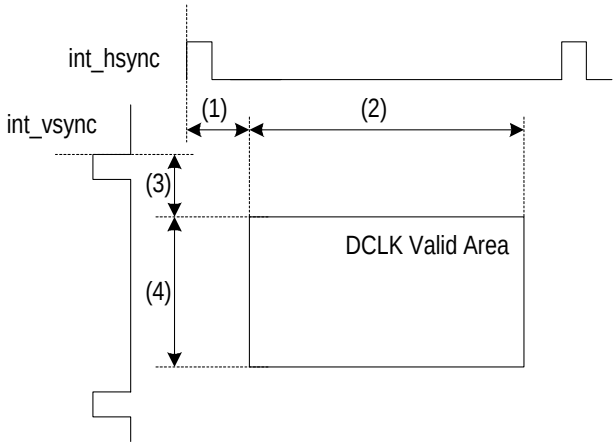


Figure 70 DCLK Pattern Register Configuration

5.5.3.2 Masking

It is possible to mask the DCLK signal in horizontal and vertical. As shown in Figure 71 , the valid start position in the horizontal direction is set relative to HSYNC, and the length of valid data in the horizontal position is set relative to the horizontal start position of valid data. The horizontal resolution is ENC clock.

The DCKME field of DCLKCTL register can activate DCLK masking. Regarding horizontal start position, two sets of registers are provided as well as pattern register.



Mark	Register	Offset	Description	Unit
(1)	DHS[12-0] DHSA[12-0]	0x22 0x23	Horizontal DCLK mask start position.	clk_enc
(2)	DHV[12-0]	0x24	Horizontal DCLK mask range.	clk_enc
(3)	DVS[12-0]	0x25	Vertical DCLK mask start position.	line
(4)	DVV[12-0]	0x26	Vertical DCLK mask range.	line

Figure 71 DCLK Masking

5.5.4 Half-rate Mode

It is possible to divide the DCLK by two. The dividing can be applied to the internal DCLK or the output DCLK. When bit DCKOH of DCLKCTL register is 1, only the DCLK output is divided by two. Since the internal DCLK is not divided, the RGB data rate is not still changed. Thus, this mode can be used to connect to the LCD that captures the data using both edges of DCLK. On the other hand, when bit DCKIH of DCLKCTL register is 1, the internal DCLK is divided by two. When output dividing is not enabled, two clocks can be output per one data. Thus this mode can be used to connect to the LCD that requires double clock frequency of data rate.

5.5.5 Line Control

The DCLK controller provides two kinds of DCLK waveform alteration by line. The culling line ID which controls RGB data output sequence also affects DCLK waveform alteration.

When bit DCKCLP of LINECTL register is 1, DCLK pattern can be switched according to the culling line ID. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.

When bit DCKCLI of LINECTL register is 1, DCLK polarity is inverted on the line whose line ID is the culling line ID set by the CULLLINE register.

Both DCKCLP and DCKCLI can be set to 1 simultaneously.

5.5.6 DCLK Output

VCLK output attributes, such as output enable, polarity and clock ouput on/off, can be controlled by VIOCTL register Moreover, the DCLK output offset can be controlled in 0.5 ENC clock unit.

5.5.7 RGB Output Formatter

5.5.7.1 RGB Filter

The RGB data from the front-end data processor can be applied to low-pass filter. The LCD controller has 3 RGB filter instances for each component R, G, B. Each component is 8bit width and filtered output is also 8bit. The filter can be a 3 tap or 7 tap filter. These can be selected by the field DFLTS of RGBCTL register. The sampling clock can also be chosen from ENC clock or its divided

clock by the bit DFLTR of RGBCTL register. Setting by DFLTS and DFLTR commonly affects three components (R, G, B).

5.5.8 YCbCr Output Formatter

YCbCr output formatter manages YCbCr data output in YCC16 and YCC8 mode.

In YCC16 mode, Y signal is output to YOUT7-0 ports at every DCLK rising edge, while Cb and Cr are alternately appeared onto COUT7-0 ports. The order of chroma output is controlled by field YCP of YCCCTL register.

In YCC8 mode, each component of YCbCr is alternately output from YOUT7-0 ports. The default output order is Cb-YCr-Y and can be modified by YCP registers. The data output is enabled only when data valid is asserted as well as RGB both in YCC16 and YCC8 mode.

ITU-R BT.656 format output is optionally available in YCC8 mode. Setting bit R656 of YCCCTL register to 1 activates this mode. In this mode, the YCbCr output timing and output order is fixed by hardware in order to conform to the standard and they cannot be altered by user. Note that this mode operates correctly only when the pixel clock frequency is half of ENC CLK.

5.5.9 Line ID Control

Line ID is the line identification flag altered at hsync and reset by vsync. This flag is used for RGB rotation order selector or DCLK waveform alteration. Normally line ID is toggled at every hsync. In addition to this normal behavior, the LCD controller provides culling line ID feature. This feature enables to use line ID toggled by specified line interval. User can also set line ID toggle position within the interval for even and odd field respectively.

The generated culling line ID affects the RGB rotation order when bit RGBCL in LINECTL register is 1. In this mode, the XORed signal of the actual line ID and the culling line ID will operate as the ID for the RGB rotation order. In addition to RGB order, DCLK waveform can be controlled by culling line ID. When DCKCLP is 1, effective DCLK pattern register is switched by the culling line ID. The DCLKPTN register is selected for culling line ID = 0 and DCLKPTNA for culling line ID =1.

DCLK inversion feature is also provided when DCKCLI=1. In this mode, the created DCLK waveform is inverted for the culling line ID=1.

5.5.10 5/6 Line Culling

The digital video output can be vertically culled of 5/6. Setting the bit VCL56 of LINECTL register to 1, can activate the culling. When in this mode, one line of video output is discarded every six lines. The VENC asserts sync for the OSD and reads data from the OSD but ignores it for output for the culled line. Hsync output and LCD_OE assertion are also disabled in the culled line. The line position to be culled can be controlled by the VCLRD and VCLID of LINECTL register. Culling is enabled on the line where the internal culling counter value is equal to VCLID. The internal culling counter is incremented at hsync and reset at vsync. The reset value can be 0 or pseudo-random value which can be selected by the VCLRD.

5.5.11 Output Hold

The LCD controller provides the video output hold function. The controller can automatically stop the operation of the timing generator at when current line or field transmission is completed. During the hold mode, reading data from the OSD is suspended and the output of sync signals and video data is also suspended. Hold function is available only for digital video output in non-standard mode.

Setting the bit HLDL of LINECTL register to 1 can bring the controller into the line hold mode. Once this register

is set, the controller automatically turns into the hold mode when current line transmission is completed. Similarly, setting the bit HLDF of LINECTL register to 1 can activate the field hold mode. After this register is set, the timing

generator is suspended at when current field transmission is completed. Setting 0 to these registers can restart the timing generator. Figure 72 and Figure 73 shows the behavior of the output hold mode.

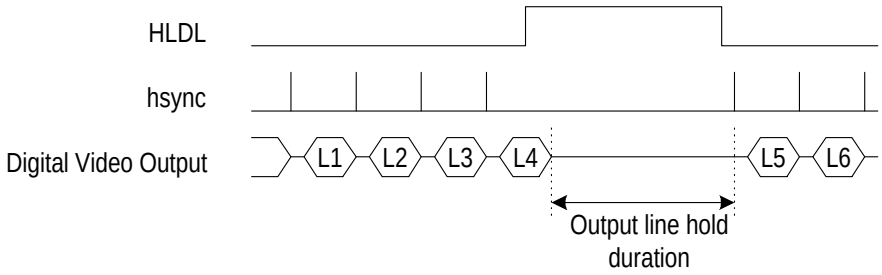


Figure 72 Output Line Hold Mode

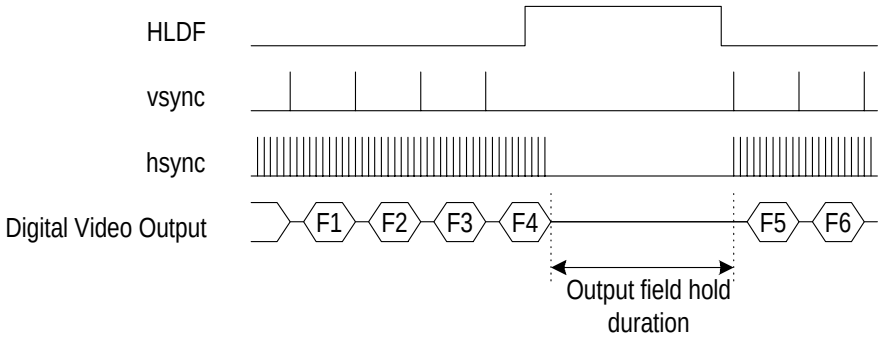


Figure 73 Output Field Hold Mode

5.5.12 GCP/FRC RAM Table

GCP/FRC table RAM of 64x16 bits is implemented by flops and it is used for the GCP pattern for EPSON D-TFD LCD panel or FRC table for STN-LCD. This RAM can be easily accessed through, RAMADR register and RAMPORT. The target RAM address (0-63) has to specified in the RAMADR register, to access the RAMPORT register which returns the contents of the specified RAM address. Writing to it overwrites the specified RAM address with the written data.

Accessing the RAMPORT automatically increments the RAMADR . The RAM contents are initialized to 0 at the reset.

5.5.13 LCD Signal Generation

BRIGHT pulse: For using BRIGHT pulse, bit BRE of LCDCTL register has to be set to 1. Polarity of this signal can be inverted by BRP in LCDCTL register. The unit is ENC clock.

LCD_AC: AC switching signal is toggled in specified field. To use LCD_AC, bit ACE of LCDCTL register has to be set to 1. The units of ACTH and ACTF are ENC clock and line respectively.

Pulse width modulation (PWM) signal: For using PWM, bit PWME of LCDCTL register has to be set to 1. Polarity can be inverted by bit PWMP in LCDCTL register. This is a free-run signal and not synchronized to any sync signals. The unit is ENC clock.

Figure 74 , Figure 75 and Figure 76 shows the timing for the BRIGHT , LCD_AC and PWM signals respectively.

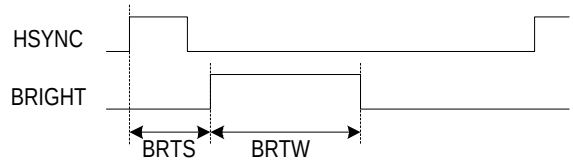


Figure 74 BRIGHT Signal Timing

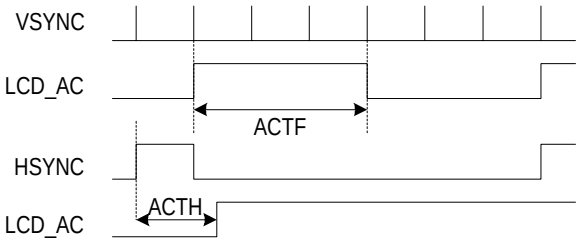


Figure 75 LCD_AC Signal Timing

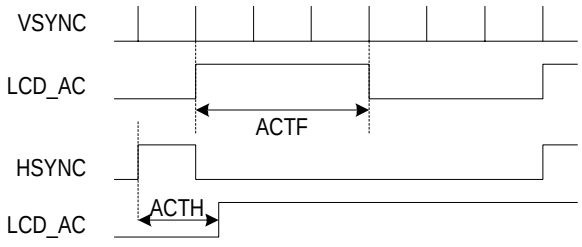


Figure 76 PWM Signal Timing

5.5.14 EPSON LCD Interface

In EPSON mode, the internal timing generator for EPSON LCD outputs timing signals. These signals can directly connect to EPSON D-TFD LCD panels. The waveform of generated timing signals is shown in Figure 77 and Figure 78. For EPSON TG signal assignment, please refer to Figure 66.

The number of low pulse of YSCL output can be one or two. One pulse is used for 1/2 reset drive type LCD, while two pulses mode is used for 1/2 select drive LCD. They can be selected by bit YSCLS of EPSON_LCDCTL register.

XINH signal has static DC output by default and its level can be set by bit XINHL of EPSON_LCDCTL register. When bit XINHS of EPSON_LCDCTL is set to 1, XINH will be controlled by internal TG. DCLK can be XSCL and it should be programmed by user appropriately. There is an option to reset vertical line counter earlier in the specified field. This function is called “SYS” (EPSON’s term). SYS can be activated by setting bit SYSE of EPSON_LCDCTL register. The effective field is set by bit SYSFID of EPSON_LCDCTL .

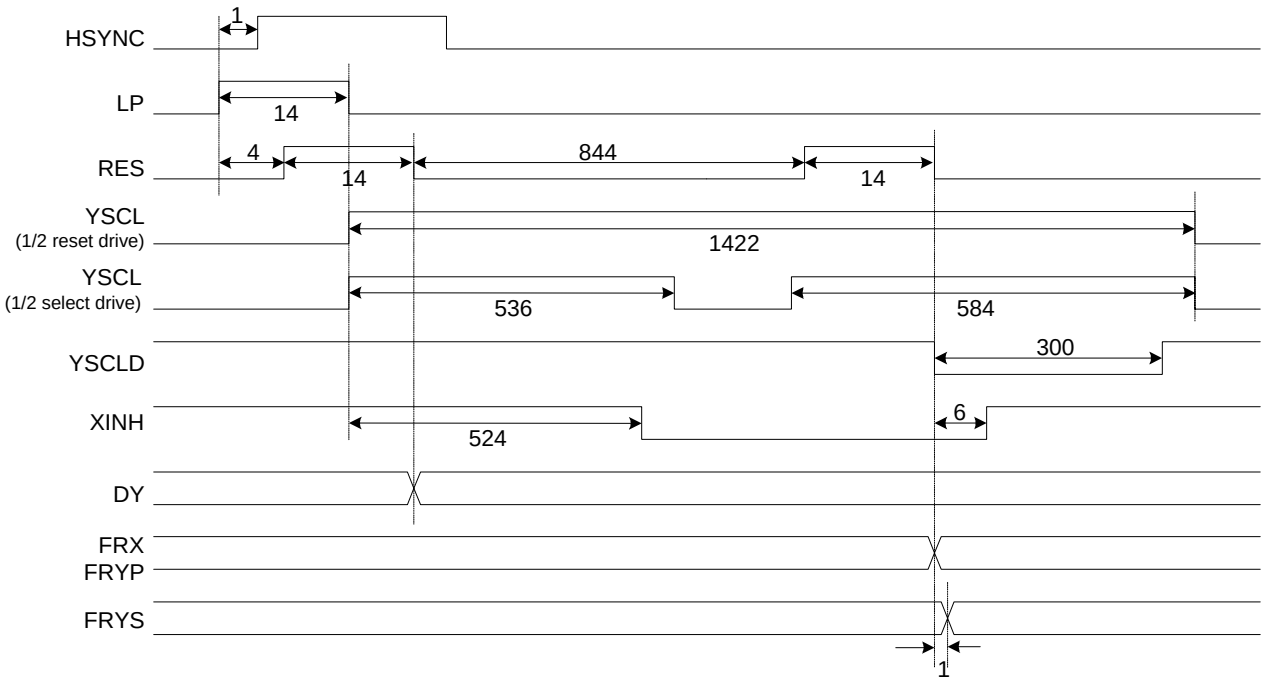


Figure 77 EPSON TG Horizontal Timing

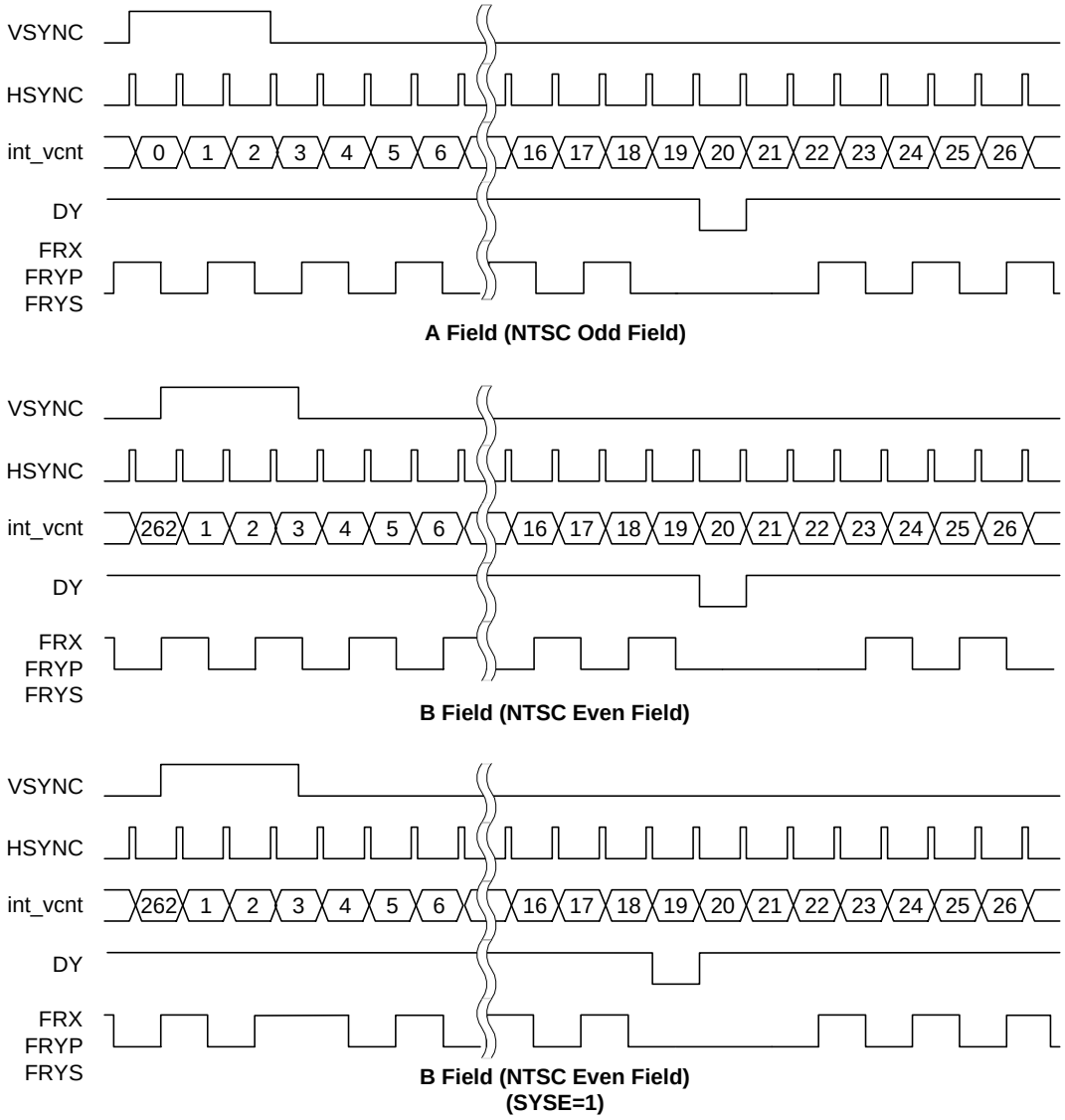


Figure 78 EPSON TG Vertical Timing

5.5.15 CASIO LCD Interface

CASIO LCD panels with serial RGB 6bit interface require the special timing signals. DM320 digital LCD controller can generate them by internal TG. The waveform is shown in Figure 79 and

Figure 80.

Line number where a GSRT pulse is asserted is determined by VSTART register setting. Horizontal timing of GSRT can be controlled by bit CDM of CASIO_LCDCTL. When CDM is 0, GSRT rises during GPCK is H. This sets the display mode to “Normal Mode”. When CDM is 1, GSRT rises before GPCK rising edge. This turns the display mode to “Vertical Reverse Mode”.

POL is toggled every line, and it is reset to the current field ID at the line specified in VSTART register. GRES is forced to L level when bit CGRES of CASIO_LCDCTL register is set to 1.

RIT port can be controlled by bit CRIT of CASIO_LCDCTL register. Update of RIT output is synchronized to the rising edge of GPCK. STBYB is controlled by bit CSTB of CASIO_LCDCTL register. The value of this bit directly output onto STBYB port. CP clock signal for charge pump is also available in CASIO mode. TG creates two clock pulses with duty 50% for every line. When CSTB is 0, CP output is automatically fixed H level.

To use CASIO panel in PAL mode, it is required to apply 5/6 line culling. When culling is applied, the appropriate lines are culled, GPCK and GRES pulses are masked on these lines. Also toggling of POL is disabled at these lines.

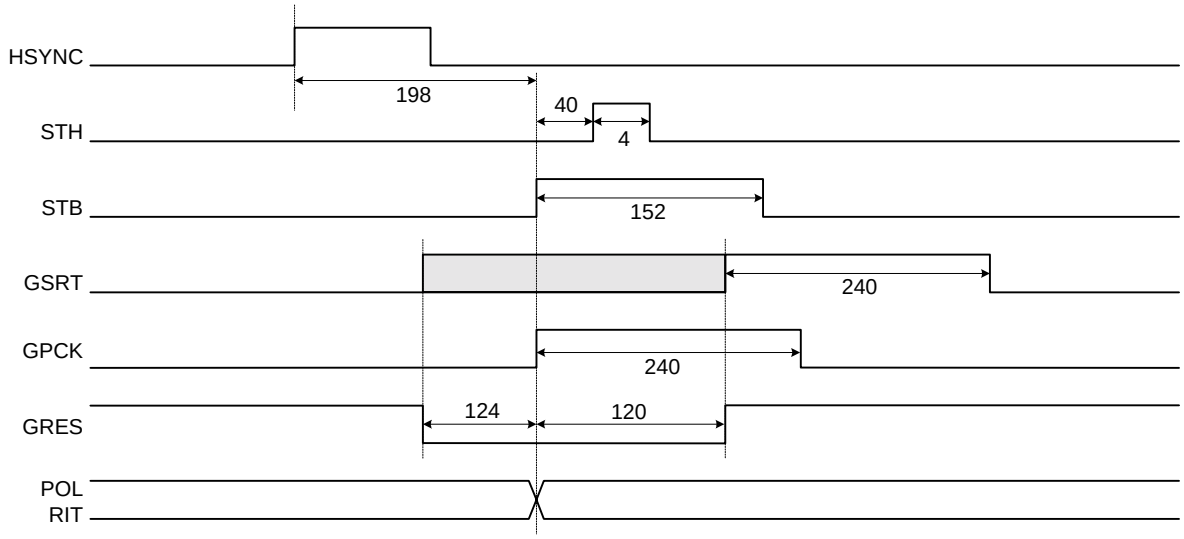


Figure 79 CASIO TG Horizontal Timing

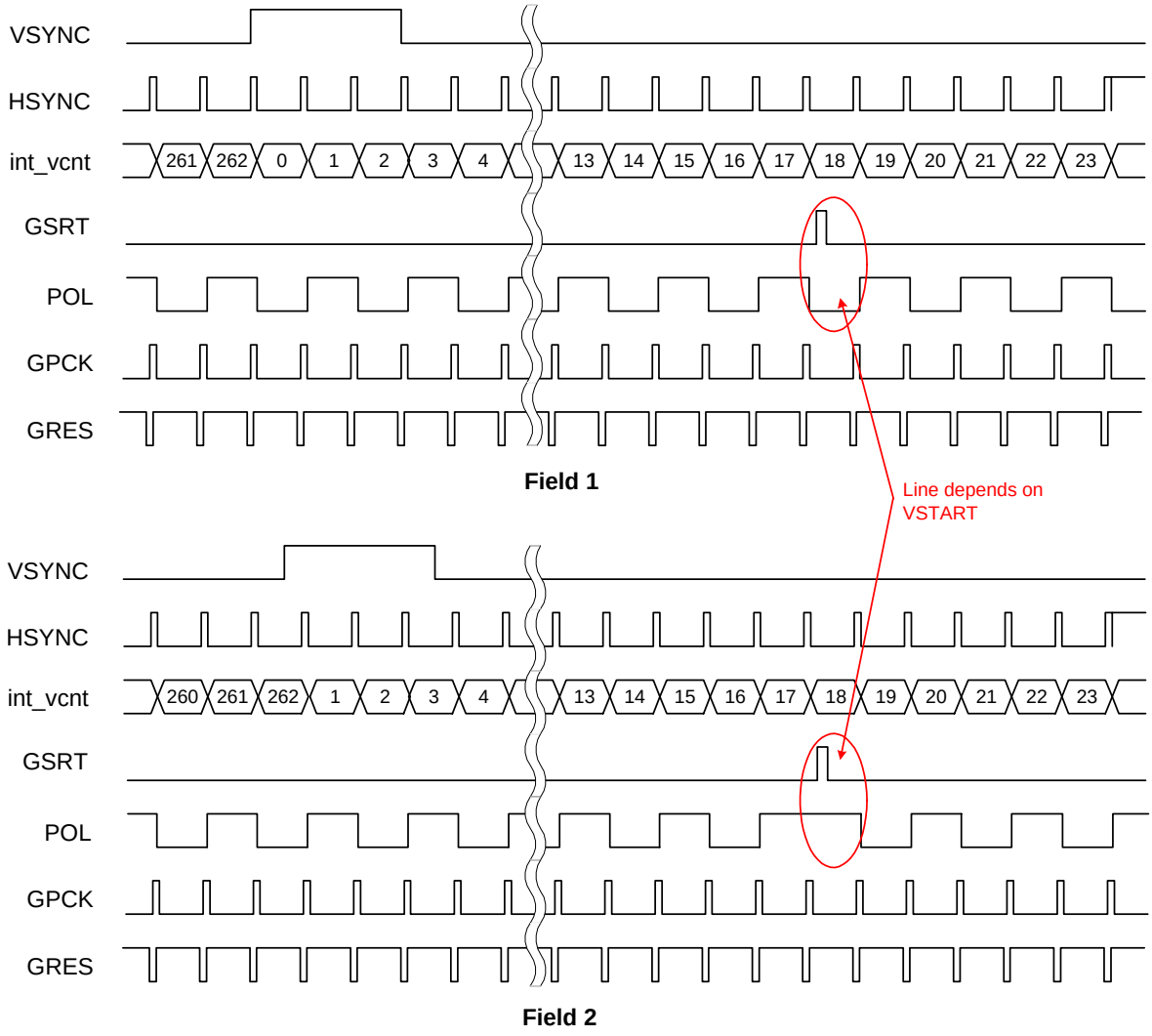


Figure 80 CASIO TG Vertical Timing

7

5.5.16 uDisplay (UDISP) Interface

DM320 LCD controller supports DisplayTech QVGA (uDisplay) interface. This is a new function in DM320. The features of uDisplay I/F are

1. Single color output during one field. RGB alteration occurs every field.

2. Monitor FULL status flag that indicates uDisplay cannot accept data, then stop data transmission while FULL is asserted.

3. Generate a FRAME_START pulse every three field.

4. Generate pingpong flag for OSD to synchronize the OSD video buffer to “field” in UDISP controller.

In UDISP mode, COUT0 and COUT1 pins are forced to input and used for FULL and BALANCE inputs respectively. There status can be monitored in UDFUL and UDBAL bits of VSTAT register.

User can change the pulse width of FRAME_START signal. Bit FSW of UDISP_LCDCTL register represents the pulse width of FRAME_START in ENC clock unit. Since FSW is set to zero by default, it should be set the appropriate number before displaying the image.

5.5.17 STN LCD Interface

STN-LCD interface is also a introduced in DM320. In STN mode, FRC (Frame Rate Control) is used for multiple tone representation. User is required to configure 16x16 FRC table. The 4 bit address corresponds to the tone of RGB data (MSB 4bit is used). The 16bit data represents dot pattern for a tone. It is shifted from MSB to LSB and circulates in period of 16 frame.

5.6 Interrupts

An interrupt pulse is asserted at every field. The internal vsync pulse triggers the interrupt assertion. Please note that it is synchronized to the internal sync timing, but not to output delayed sync or OSD sync. Figure 81 shows the detail interrupt generation.

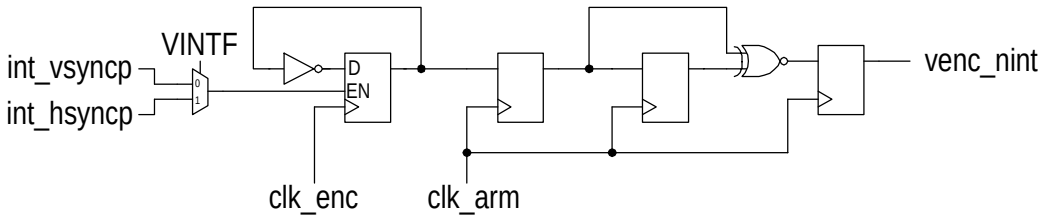


Figure 81 Interrupt Generation Circuit

5.7 DAC Control

There are a several registers that control the embedded DAC macro (DAA15). To power down DAC itself, bit DAPD of VMOD register should be set to 1. By default, this bit is set to 1, so user has to write 0 before using analog output. To get DC output from DAOUT pin, DC output mode is useful. Setting DADC bit of DACTST register to 1 switches DAC digital input from normal video signal to value of DALVL bit in DACTST register . Bit DAOE of DACTST register can control the OE signal of DAA15. When set to 1, DAOUT output is fixed to L level.

5.8 Video Encoder Register Map (VENC)

Address	Register	Description
0003:0800	VMOD	Video Mode
0003:0802	VIDCTL	Video interface I/O control
0003:0804	VDPRO	Video data processing
0003:0806	SYNCCTL	Sync control
0003:0808	HSPLS	Horizontal Sync pulse width
0003:080A	VSPLS	Vertical Sync pulse width
0003:080C	HINT	Horizontal interval
0003:080E	HSTART	Horizontal valid data start position
0003:0810	HVALID	Horizontal data valid range
0003:0812	VINT	Vertical interval
0003:0814	VSTART	Vertical valid data start position
0003:0816	VVALID	Vertical data valid range
0003:0818	HSDLY	Horizontal sync delay
0003:081A	VSDLY	Vertical sync delay
0003:081C	YCCCTL	YCbCr control
0003:081E	RGBCTL	RGB control
0003:0820	RGBCLP	RGB level clipping
0003:0822	LINECTL	Line Id control
0003:0824	CULLLINE	Culling line control
0003:0826	LCDOUT	LCD output signal control
0003:0828	BRTS	Brightness start position signal control
0003:082A	BRTW	Brightness width signal control
0003:082C	ACCTL	LCD_AC signal control
0003:082E	PWMP	PWM start position signal control
0003:0830	PWMW	PWM width signal control
0003:0832	DCLKCTL	DCLK control
0003:0834	DCLKPTN0	DCLK pattern 0
0003:0836	DCLKPTN1	DCLK pattern 1
0003:0838	DCLKPTN2	DCLK pattern 2
0003:083A	DCLKPTN3	DCLK pattern 3
0003:083C	DCLKPTN0A	DCLK auxiliary pattern 0
0003:083E	DCLKPTN1A	DCLK auxiliary pattern 1
0003:0840	DCLKPTN2A	DCLK auxiliary pattern 2
0003:0842	DCLKPTN3A	DCLK auxiliary pattern 3
0003:0844	DCLKHS	Horizontal DCLK mask start
0003:0846	DCLKHSA	Horizontal auxiliary DCLK mask start
0003:0848	DCLKHR	Horizontal DCLK mask range
0003:084A	DCLKVS	Vertical DCLK mask start
0003:084C	DCLKVR	Vertical DCLK mask range
0003:084E	CAPCTL	Closed caption control
0003:0850	CAPDO	Closed caption odd field data
0003:0852	CAPDE	Closed caption even field data
0003:0854	ATR0	Video Attribute Data #0

0003:0856	ATR1	Video Attribute Data #1
0003:0858	ATR2	Video Attribute Data #2
0003:085A	EPSON_LCDCTL	EPSON LCD Control
0003:085A	CASIO_LCDCTL	CASIO LCD Control
0003:085A	UDISP_LCDCTL	uDisplay LCD control
0003:085A	STN_LCDCTL	STN LCD control
0003:085C	VSTAT	Video status
0003:085E	RAMADR	GCP/FRC table RAM address
0003:0860	RAMPORT	GCP/FRC table RAM data port
0003:0862	DACTST	DAC Test
0003:0864	YCOLVL	YOUT and COUT levels
0003:0866	SCPROG	Sub-carrier programming

5.9 Video Encoder Interface Registers

5.9.1 VMOD

Video Mode Setup Register

VMOD 0003:0800 offset: 0x00 default: 0x0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	VDMD[2]	VDMD[1]	VDMD[0]	RSV	ITLC	CBTYP	CBMD	NTPLS[1]	NTPLS[0]	SLAVE	VMD	BLNK	DACPD	VIE	VENC
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	-	0	0	0	0	0	0	0	0	1	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:12	VDMD	0	R/W	Digital video output mode » 0: YCbCr parallel 16 bit « » 1: YCbCr serial 8 bit « » 2: RGB666 parallel 18 bit « » 3: RGB8 serial 8 bit « » 4: EPSON « » 5: CASIO « » 6: uDISP (QVGA uDisplay) « » 7: STN (STN-LCD) «
11	RSV			Reserved
10	ITLC	0	R/W	Scan Mode » 0: Interlace « » 1: Non-interlace « Note: This setting is effective in standard mode (VMD=0)
9	CBTYP	0	R/W	Color Bar Type » 0: 75% « » 1: 100% «
8	CBMD	0	R/W	Color bar mode » 0: Normal output « » 1: Color bar output «
7:6	NTPLS	0	R/W	NTSC / PAL mode select » 0: NTSC « » 1: PAL « » 2: Reserved « » 3: Reserved «
5	SLAVE	0	R/W	Master-slave select.Set “1” to operate this module in slave mode in synchronization with external sync signal or CCDC sync signal » 0: Master mode « » 1: Slave mode «
4	VMD	0	R/W	Video timing » 0: NTSC/PAL timing « » 1: Not NTSC/PAL timing «
3	BLNK	0	R/W	Blanking enable » 0: Normal « » 1: Force Blanking «
2	DACPD	1	R/W	DAC Powerdown » 0: Normal mode« » 1: Powerdown mode «
1	VIE	0	R/W	Composite output enable » 0: Fixed L level output « » 1: Normal composite output «
0	VENC	0	R/W	Video Encoder Enable » 0: Disable « » 1: Enable «

5.9.2 VIOCTL

Video I/O Control Register

VIDCTL 0003:0802 offset: 0x02 default: 0x1001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	VCLKP	VCLKE	VCLKZ	RSV	RSV	RSV	RSV	RSV	RSV	DOMD[1]	DOMD[0]	RSV	YCDC	INPTRU	YCDIR
R/W	-	R/W	R/W	R/W	-	-	-	-	-	-	R/W	R/W	-	R/W	R/W	R/W
Default	-	0	0	1	-	-	-	-	-	-	0	0	-	0	0	1

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14	VCLKP	0	R/W	VCLK output polarity » 0: Non-inverse « » 1: Inverse «
13	VCLKE	0	R/W	VCLK output enable » 0: Off « » 1: On « Note: Setting 1 outputs DCLK from VCLK pin. When 0 VCLKP setting is still available
12	VCLKZ	1	R/W	VCLK pin output enable » 0: Output « » 1: High Impedence «
11:6	RSV			Reserved
5:4	DOMD	0	R/W	Digital data output mode » 0: Normal output « » 1: Inverse output « » 2: L level output « » 3: H level output «
3	RSV			Reserved
2	YCDC	0	R/W	YOUT/COUT pin DC output mode » 0: Normal output « » 1: DC level output «
1	INPTRU	0	R/W	YOUT / COUT pin output mode » 0: Digital video output « » 1: YIN / CIN input through «
0	YCDIR	1	R/W	YOUT / COUT pin I/O control » 0: Output « » 1: Input « Note: YOUT/COUT pin is used as YC data input pin for CCDC. Set '0' for digital video output

5.9.3 VDPRO

Video Data Processing Register

VDPRO 0003:0804 offset: 0x04 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PFLTC[1]	PFLTC[0]	PFLTY[1]	PFLTY[0]	PFLTR	YCDLY[2]	YCDLY[1]	YCDLY[0]	RGBMAT	ATRGB	ATYCC	ATCOM	STUP	CRCUT	CUPS	YUPS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:14	PFLTC	0	R/W	C Prefilter select » 0: No filter « » 1: 1+1 « » 2: 1+2+1 « » 3: Reserved « Note: When PFLTR and PFLTY are '1', set PFLTY to 1 tp adjust delay between Y and C.
13:12	PFLTY	0	R/W	Y Prefilter select » 0: No filter « » 1: 1+1 « » 2: 1+2+1 « » 3: Reserved «
11	PFLTR	0	R/W	Prefilter sampling frequency » 0: ENC clock / 2 « » 1: ENC clock «
10:8	YCDLY	0	R/W	Delay adjsutment of Y signal in composite signal This is set by ENC clock » 0: 0 « » 1: +1 « » 2: +2 « » 3: +3 « » 4: -4 « » 5: -3 « » 6: -2 « » 7: -1 « Note: The value is 2's complement
7	RGBMAT	0	R/W	RGB conversion matrix (YCbCr - RGB) 0: 1/512 | R = 596 0 816 Y-16 | | G = 596 -199 -414 Cb-128 | | B = 596 1029 0 Cr-128 | 1: 1/512 | R = 512 0 718 Y | | G = 512 -176 -366 Cb-128 | | B = 512 907 0 Cr-128 |
6	ATRGB	0	R/W	Input video Attenuation control for RGB » 0: No Attenuation « » 1: 0-255 -> REC601 specified level
5	ATYCC	0	R/W	Input video Attenuation control for YCbCr » 0: No Attenuation « » 1: 0-255 -> REC601 specified level
4	ATCOM	0	R/W	Input video data damping control (for composite output) » 0: No Attenuation « » 1: 0-255 -> REC601 specified level
3	STUP	0	R/W	Setup level at NTSC output » 0: 0% « » 1: 7.5% «
2	CRCUT	0	R/W	Chroma signal low pass filter select » 0: 1.5 MHz cut-0ff« » 1: 3 MHz cut-off «
1	CUPS	0	R/W	Chroma signal up sampling enable » 0: Off « » 1: On «
0	YUPS	0	R/W	Y signal up sampling enable » 0: Off « » 1: On «

5.9.4 SYNCTL

Sync Control Register

SYNCCTL 0003:0806 offset: 0x06 default: 0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	EXFEN	EXFIV	EXCCD	EXVIV	EXHIV	CSP	CSE	SYSW	VSYNCS	VPL	HPL	SYE	SYDIR
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12	EXFEN	0	R/W	External field input mode Effective in slave operation (SLAVE=1). When this bit is at "1" and "EXCCD=1", the field signal generated in CCDC module is used as external field input, and at "1" and "EXCCD=0", the field is fixed "0". When this is set at "0", field ID generated internally is used » 0: Internal field mode « » 1: External field mode «
11	EXFIV	0	R/W	External field input inversion, effective in slave operation » 0: Non-inverse « » 1: Inverse «
10	EXCCD	0	R/W	External sync select, effective in slave operation » 0: HSYNC/VSYNC pin « » 1: CCD sync signal «
9	EXVIV	0	R/W	External vertical sync input polarity » 0: Active H « » 1: Active L «
8	EXHIV	0	R/W	External horizontal sync input polarity » 0: Active H « » 1: Active L «
7	CSP	0	R/W	Composite sync output polarity » 0: Active H « » 1: Active L « Note: Specifies polarity of composite sync output from COUT3 pin in YCC8 or RGB8 mode
6	CSE	0	R/W	Composite sync output enable » 0: Off « » 1: On « Note: Output control of composite sync signal from COUT3 pin in YCC8 or RGB8 mode. Writing 1 activates output, and writing 0 outputs inactive level determined by CSP
5	SYSW	0	R/W	Output sync select » 0: Normal « » 1: Sync pulse width processing mode« Note: Applicable to Standard mode only
4	VSYNCS	0	R/W	VSYNC pin output signal select » 0: Vertical sync signal « » 1: composite sync signal «
3	VPL	0	R/W	Vertical sync output polarity » 0: Active H « » 1: Active L «
2	HPL	0	R/W	Horizontal sync output polarity » 0: Active H « » 1: Active L «
1	SYE	0	R/W	Sync output enable » 0: Off « » 1: On «
0	SYDIR	1	R/W	Horizontal / Vertical pin I/O control » 0: Output « » 1: Input «

5.9.5 HSPLS

Horizontal Sync Pulse Width Register

HSPLS 0003:0808 offset: 0x08 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	HSPLS[12]	HSPLS[11]	HSPLS[10]	HSPLS[9]	HSPLS[8]	HSPLS[7]	HSPLS[6]	HSPLS[5]	HSPLS[4]	HSPLS[3]	HSPLS[2]	HSPLS[1]	HSPLS[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	HSPLS	0	R/W	Horizontal sync pulse width. Set the pulse width of horizontal sync output from HSYNC pin in ENC clock. Effective in non-standard mode, or sync processing mode (SYSW=1) in standard mode

5.9.6 VSPLS

Vertical Sync Pulse Width Register

VSPLS 0003:080A offset: 0x0A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	VSPLS[12]	VSPLS[11]	VSPLS[10]	VSPLS[9]	VSPLS[8]	VSPLS[7]	VSPLS[6]	VSPLS[5]	VSPLS[4]	VSPLS[3]	VSPLS[2]	VSPLS[1]	VSPLS[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	VSPLS	0	R/W	Vertical sync pulse width. Set the pulse width of vertical sync output from VSYNC pin in lines. Effective in non-standard mode, or sync processing mode (SYSW=1) in standard mode

5.9.7 HINT

Horizontal Interval Register

HINT 0003:080C offset: 0x0C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	HINT[12]	HINT[11]	HINT[10]	HINT[9]	HINT[8]	HINT[7]	HINT[6]	HINT[5]	HINT[4]	HINT[3]	HINT[2]	HINT[1]	HINT[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	HINT	0	R/W	Horizontal interval. Effective in non-standard mode. Specify the number of ENC clocks. The interval is represented by HINT+1. If ENC clock/2 is used as OSD clock, ensure that even value is specified

5.9.8 HSTART

Horizontal Valid Data Start Position

HSTART 0003:080E offset: 0x0E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	HSTART[12]	HSTART[11]	HSTART[10]	HSTART[9]	HSTART[8]	HSTART[7]	HSTART[6]	HSTART[5]	HSTART[4]	HSTART[3]	HSTART[2]	HSTART[1]	HSTART[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	HSTART	0	R/W	Horizontal data valid start position. Specify the number of ENC clocks from horizontal sync signal. LCD_OE rises at the position specified here and the data output starts

5.9.9 HVALID

Horizontal Data Valid Range

HVALID 0003:0810 offset: 0x10 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	HVALID[12]	HVALID[11]	HVALID[10]	HVALID[9]	HVALID[8]	HVALID[7]	HVALID[6]	HVALID[5]	HVALID[4]	HVALID[3]	HVALID[2]	HVALID[1]	HVALID[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	HVALID	0	R/W	Horizontal data valid range Specify the number of ENC clocks. LCD_OE is asserted during the period specified here and valid data is output. The data outside of valid range is output in L

5.9.10 VINT

Vertical Interval

VINT 0003:0812 offset: 0x12 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	VINT[12]	VINT[11]	VINT[10]	VINT[9]	VINT[8]	VINT[7]	VINT[6]	VINT[5]	VINT[4]	VINT[3]	VINT[2]	VINT[1]	VINT[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	VINT	0	R/W	Vertical interval. Effective in non-standard mode. Specify the number of lines. The interval is represented by VINT+1

5.9.11 VSTART

Vertical Data Valid Start Position

VSTART 0003:0814 offset: 0x14 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	VSTART[12]	VSTART[11]	VSTART[10]	VSTART[9]	VSTART[8]	VSTART[7]	VSTART[6]	VSTART[5]	VSTART[4]	VSTART[3]	VSTART[2]	VSTART[1]	VSTART[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	VSTART	0	R/W	Vertical valid data start position Note: Specify number of lines

5.9.12 VVALID

Vertical Valid Data Range

VVALID 0003:0816 offset: 0x16 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	VVALID[12]	VVALID[11]	VVALID[10]	VVALID[9]	VVALID[8]	VVALID[7]	VVALID[6]	VVALID[5]	VVALID[4]	VVALID[3]	VVALID[2]	VVALID[1]	VVALID[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	VVALID	0	R/W	Vertical data valid range Note: specify number of lines

5.9.13 HSDLY

Horizontal Sync Delay Register

HSDLY 0003:0818 offset: 0x18 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	HSDLY[12]	HSDLY[11]	HSDLY[10]	HSDLY[9]	HSDLY[8]	HSDLY[7]	HSDLY[6]	HSDLY[5]	HSDLY[4]	HSDLY[3]	HSDLY[2]	HSDLY[1]	HSDLY[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	HSDLY	0	R/W	Output delay of horizontal sync signal. This can delay horizontal sync output from HSYNC pin by ENC clock

5.9.14 VSDLY

Vertical Sync Delay Register

VSDLY 0003:081A offset: 0x1A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	VSDLY[12]	VSDLY[11]	VSDLY[10]	VSDLY[9]	VSDLY[8]	VSDLY[7]	VSDLY[6]	VSDLY[5]	VSDLY[4]	VSDLY[3]	VSDLY[2]	VSDLY[1]	VSDLY[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	VSDLY	0	R/W	Output delay of vertical sync signal Note: This will delay the VSYNC signal by ENC clock

5.9.15 YCCCTL

YcbCr Control Register

YCCCTL 0003:081C offset: 0x1C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	YCP[1]	YCP[0]	RSV	R656
R/W	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W	-	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0

Bit	Name	Reset Value	R/W	Function
15:4	RSV			Reserved
3:2	YCP	0	R/W	YC output order YCC16 mode » 0: CbCr « » 1: CrCb « » 2: Reserved « » 3: Reserved « YCC8 mode » 0: Cb-Y-Cr-Y « » 1: Y-Cr-Y-Cb « » 2: Cr-Y-Cb-Y « » 3: Y-Cb-Y-Cr «
1	RSV			Reserved
0	R656	0	R/W	REC656 mode » 0: Normal « » 1: REC656 mode « Note: This is effective in YCC8 mode

5.9.16 RGBCTL

RGB Control Register

RGBCTL 0003:081E offset: 0x1E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	IRONM	DFLTR	DFLTS[1]	DFLTS[0]	RSV	RGBEF[2]	RGBEF[1]	RGBEF[0]	RSV	RGBOF[2]	RGBOF[1]	RGBOF[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	-	0	0	0	-	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11	IRONM	0	R/W	Iron-man type RGB output » 0: Normal « » 1: Iron-man type «
10	DFLTR	0	R/W	RGB LPF sampling frequency » 0: ENC clock / 2 « » 1: ENC clock « Note: Effective in all digital modes with RGB output
9:8	DFLTS	0	R/W	RGB LPF select » 0: No filter « » 1: 1+2+1 « » 2: 1+2+3+4+3+2+1 « » 3: Reserved « Note: Effective in all digital modes with RGB output
7	RSV			Reserved
6:4	RGBEF	0	R/W	RGB output order (Line Id = 1) » 0: R0-G1-B2 « » 1: R0-B1-G2 « » 2: G0-R1-B2 « » 3: G0-B1-R2 « » 4: B0-R1-G2 « » 5: B0-G1-R2 « » 6: Reserved « » 7: Reserved « Note: Effective in RGB8, EPSON and CASIO modes
3	RSV			Reserved
2:0	RGBOF	0	R/W	RGB output order (Line Id = 0) » 0: R0-G1-B2 « » 1: R0-B1-G2 « » 2: G0-R1-B2 « » 3: G0-B1-R2 « » 4: B0-R1-G2 « » 5: B0-G1-R2 « » 6: Reserved « » 7: Reserved « Note: Effective in RGB8, EPSON and CASIO modes

5.9.17 RGBCLP

RGB Level Clipping Register

RGBCLP 0003:0820 offset: 0x20 default: 0xFF00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UCLIP[7]	UCLIP[6]	UCLIP[5]	UCLIP[4]	UCLIP[3]	UCLIP[2]	UCLIP[1]	UCLIP[0]	OFST[7]	OFST[6]	OFST[5]	OFST[4]	OFST[3]	OFST[2]	OFST[1]	OFST[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	UCLP	255	R/W	Upper clip level for RGB output Note: Effective in all digital output modes with RGB output. Clipping is done following offset addition
7:0	OFST	0	R/W	Offset level for RGB output Note: Effective in all digital output modes with RGB output. Offset specified here can be added to RGB converted from YCbCr

5.9.18 LINECTL

Line Id Control Register

LINECTL 0003:0822 offset: 0x22 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXIDP	EXIDE	RSV	RSV	RSV	VCLID[2]	VCLID[1]	VCLID[0]	VCLRD	VCL56	HLDF	HLDL	LINID	DCKCLP	DCKCLI	RGBCL
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	EXDP	0	R/W	External Line Id signal polarity » 0: Non-inverse « » 1: Inverse «
14	EXDE	0	R/W	External Line Id signal input mode » 0: Internal Id line « » 1: External Id Line «
13:11	RSV			Reserved
10:8	VCLID	0	R/W	Vertical Culling line position Effective when VCL56 = 1. No culling when VCLID > 5 Note: This setting is effective if VCL56 = 1
7	VCLRD	0	R/W	Vertical Culling counter reset mode » 0: Reset to 0 « » 1: Reset to Random value «
6	VCL56	0	R/W	Digital output vertical culling of 5/6 » 0: No culling « » 1: 5/6 culling «
5	HLDF	0	R/W	Digital output Field Hold » 0: Normal « » 1: Output hold « Note: Effective in non-standard mode
4	HLDL	0	R/W	Digital output Line Hold » 0: Normal « » 1: Output hold « Note: Effective in non-standard mode
3	LINID	0	R/W	Start line Id control in even field » 0: Line Id=0 « » 1: Line Id=1 «
2	DCKCLP	0	R/W	DCLK pattern switching by culling line Id » 0: Off « » 1: On «
1	DCKCLI	0	R/W	DCLK polarity inversion by culling line Id » 0: Off « » 1: On «
0	RGBCL	0	R/W	RGB output order switching by culling line Id » 0: Off « » 1: On «

5.9.19 CULLLINE

Culling Line control

CULLLINE 0003:0824 offset: 0x24 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLOF[3]	CLOF[2]	CLOF[1]	CLOF[0]	CLEF[3]	CLEF[2]	CLEF[1]	CLEF[0]	RSV	RSV	RSV	RSV	CULI[3]	CULI[2]	CULI[1]	CULI[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-	-	-	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	CLOF	0	R/W	Culling line Id toggle position (Odd field) Specify toggle line numbers of culling line ID in odd field
11:8	CLEF	0	R/W	Culling line Id toggle position (Even field) Specify the culling line ID toggle position in even field
7:4	RSV			Reserved
3:0	CULI	0	R/W	Culling line Id inversion interval This is set by line. The interval is represented by CULI+1

5.9.20 LCDOUT

LCD Output Signal Control Register

LCDOUT 0003:0826 offset: 0x26 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	FIDS	FIDP	PWMP	PWME	ACE	BRP	BRE	OEP	OEE
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:9	RSV			Reserved
8	FIDS	0	R/W	GIO39 output signal select » 0: Field Id « » 1: LCD_OE « Note: Select GIO39 signal using FSEL3[13:12] = 01
7	FIDP	0	R/W	Field Id output polarity » 0: Non-inverse « » 1: Inverse «
6	PWMP	0	R/W	PWM output pulse polarity » 0: Active H « » 1: Active L «
5	PWME	0	R/W	PWM output control, effective when digital output mode with PWM output is selected » 0: Off « » 1: On «
4	ACE	0	R/W	LCD_AC output control » 0: Off « » 1: On «
3	BRP	0	R/W	Bright output polarity » 0: Active H « » 1: Active L «
2	BRE	0	R/W	Bright output control » 0: Off « » 1: On «
1	OEP	0	R/W	LCD_OE output polarity » 0: Active H « » 1: Active L «
0	OEE	0	R/W	LCD_OE output control » 0: Off « » 1: On «

5.9.21 BRTS

Brightness Start Position Signal Control Register

BRTS 0003:0828 offset: 0x28 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	BRTS[12]	BRTS[11]	BRTS[10]	BRTS[9]	BRTS[8]	BRTS[7]	BRTS[6]	BRTS[5]	BRTS[4]	BRTS[3]	BRTS[2]	BRTS[1]	BRTS[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	BRTS	0	R/W	Bright pulse start position Specify the number of ENC cycles from HSYNC signal.

5.9.22 BRTW

Brightness Width Signal Control Register

BRTW 0003:082A offset: 0x2A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	BRTW[12]	BRTW[11]	BRTW[10]	BRTW[9]	BRTW[8]	BRTW[7]	BRTW[6]	BRTW[5]	BRTW[4]	BRTW[3]	BRTW[2]	BRTW[1]	BRTW[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	BRTW	0	R/W	Bright pulse width Specify the number of ENC cycles.

5.9.23 ACCTL

LCD_AC signal Control Register

ACCTL 0003:082C offset: 0x2C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACTF[2]	ACTF[1]	ACTF[0]	ACTH[12]	ACTH[11]	ACTH[10]	ACTH[9]	ACTH[8]	ACTH[7]	ACTH[6]	ACTH[5]	ACTH[4]	ACTH[3]	ACTH[2]	ACTH[1]	ACTH[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	ACTF	0	R/W	LCD_AC toggle interval Note: LCD_AC is toggled every field specified here
12:0	ACTH	0	R/W	LCD_AC toggle horizontal position Note: LCD_AC is toggled by the number of ENC clocks from the rising edge of horizontal sync signal

5.9.24 PWMP

Pulse Width Modulator Start Position Signal Control Register

PWMP 0003:082E offset: 0x2E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	PWMP[12]	PWMP[11]	PWMP[10]	PWMP[9]	PWMP[8]	PWMP[7]	PWMP[6]	PWMP[5]	PWMP[4]	PWMP[3]	PWMP[2]	PWMP[1]	PWMP[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	PWMP	0	R/W	PWM output period Specify the number of ENC clocks. Period is PWMP + 1

5.9.25 PWMW

Pulse Width Modulator Start Width Signal Control Register

PWMW 0003:0830 offset: 0x30 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	PWMW[12]	PWMW[11]	PWMW[10]	PWMW[9]	PWMW[8]	PWMW[7]	PWMW[6]	PWMW[5]	PWMW[4]	PWMW[3]	PWMW[2]	PWMW[1]	PWMW[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	PWMW	0	R/W	PWM output pulse width Specify the H pulse width by ENC clock. Setting '0' makes PWM output L level always, Setting bigger value than PWMP sets to H level always,

5.9.26 DCLKCTL

DCLK Control Register

DCLKCTL 0003:0832 offset: 0x32 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	DOFST[1]	DOFST[0]	DCKEC	DCKME	DCKOH	DCKIH	RSV	RSV	DCKPW[5]	DCKPW[4]	DCKPW[3]	DCKPW[2]	DCKPW[1]	DCKPW[0]
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	0	0	0	0	0	-	-	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:11	RSV			Reserved
13:12	DOFST	0	R/W	DCLK output offset 0: 0 1: -0.5 2: +0.5 3: +1.0 To adjust the DCLK delay from VCLK pin by ENC clock.
11	DCKEC	0	R/W	DCLK Pattern mode » 0: Level « » 1: Enable « When 0, the specified value in DCLKPTN (or DCLKPTNA) register becomes the clock level of DCLK. When 1, DCLKPTN works as the clock enable for ENC clock
10	DCKME	0	R/W	DCLK mask control » 0: Off « » 1: On « Note: Setting '1' means mask is on and setting '0' means mask is off
9	DCKOH	0	R/W	DCLK output dividing control » 0: Divide by 1 « » 1: Divide by 2«
8	DCKIH	0	R/W	Internal DCLK dividing control » 0: Divide by 1 « » 1: Divide by 2«
7:6	RSV			Reserved
5:0	DCKPW	0	R/W	DCLK pattern valid bit width Note: Set the width of valid bits among all 64 bits in the DCLKPTN0-3 registers

5.9.27 DCLKPTN0

DCLK Pattern 0 Register

DCLKPTN0 0003:0834 offset: 0x34 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN0[15]	DCPTN0[14]	DCPTN0[13]	DCPTN0[12]	DCPTN0[11]	DCPTN0[10]	DCPTN0[9]	DCPTN0[8]	DCPTN0[7]	DCPTN0[6]	DCPTN0[5]	DCPTN0[4]	DCPTN0[3]	DCPTN0[2]	DCPTN0[1]	DCPTN0[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN0	0	R/W	DCLK pattern(DCPT15-DCPT0) The specified bit pattern is output in resolution of ENC clock units

5.9.28 DCLKPTN1

DCLK Pattern 1 Register

DCLKPTN1 0003:0836 offset: 0x36 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN1[15]	DCPTN1[14]	DCPTN1[13]	DCPTN1[12]	DCPTN1[11]	DCPTN1[10]	DCPTN1[9]	DCPTN1[8]	DCPTN1[7]	DCPTN1[6]	DCPTN1[5]	DCPTN1[4]	DCPTN1[3]	DCPTN1[2]	DCPTN1[1]	DCPTN1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN1	0	R/W	DCLK pattern (DCPT31-DCPT16) The specified bit pattern is output in resolution of ENC clock units

5.9.29 DCLKPTN2

DCLK Pattern 2 Register

DCLKPTN2 0003:0838 offset: 0x38 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN2[15]	DCPTN2[14]	DCPTN2[13]	DCPTN2[12]	DCPTN2[11]	DCPTN2[10]	DCPTN2[9]	DCPTN2[8]	DCPTN2[7]	DCPTN2[6]	DCPTN2[5]	DCPTN2[4]	DCPTN2[3]	DCPTN2[2]	DCPTN2[1]	DCPTN2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN2	0	R/W	DCLK pattern (DCPT47-DCPT32) The specified bit pattern is output in resolution of ENC clock units

5.9.30 DCLKPTN3

DCLK Pattern 3 Register

DCLKPTN3 0003:083A offset: 0x3A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN3[15]	DCPTN3[14]	DCPTN3[13]	DCPTN3[12]	DCPTN3[11]	DCPTN3[10]	DCPTN3[9]	DCPTN3[8]	DCPTN3[7]	DCPTN3[6]	DCPTN3[5]	DCPTN3[4]	DCPTN3[3]	DCPTN3[2]	DCPTN3[1]	DCPTN3[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN3	0	R/W	DCLK pattern (DCPT63-DCPT48) The specified bit pattern is output in resolution of ENC clock units

5.9.31 DCLKPTN0A

DCLK Auxiliary Pattern 0 Register

DCLKPTN0A 0003:083C offset: 0x3C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN0A[15]	DCPTN0A[14]	DCPTN0A[13]	DCPTN0A[12]	DCPTN0A[11]	DCPTN0A[10]	DCPTN0A[9]	DCPTN0A[8]	DCPTN0A[7]	DCPTN0A[6]	DCPTN0A[5]	DCPTN0A[4]	DCPTN0A[3]	DCPTN0A[2]	DCPTN0A[1]	DCPTN0A[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN0A	0	R/W	DCLK pattern (DCPTA15-DCPTA0) auxiliary The specified bit pattern is output in resolution of ENC clock units

5.9.32 DCLKPTN1A

DCLK Auxiliary Pattern 1 Register

DCLKPTN1A 0003:083E offset: 0x3E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN1A[15]	DCPTN1A[14]	DCPTN1A[13]	DCPTN1A[12]	DCPTN1A[11]	DCPTN1A[10]	DCPTN1A[9]	DCPTN1A[8]	DCPTN1A[7]	DCPTN1A[6]	DCPTN1A[5]	DCPTN1A[4]	DCPTN1A[3]	DCPTN1A[2]	DCPTN1A[1]	DCPTN1A[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN1A	0	R/W	DCLK pattern (DCPTA31-DCPTA16)auxiliary The specified bit pattern is output in resolution of ENC clock units

5.9.33 DCLKPTN2A

DCLK Auxiliary Pattern 2 Register

DCLKPTN2A 0003:0840 offset: 0x40 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPTN2A[15	CPTN2A[14	CPTN2A[13	CPTN2A[12	CPTN2A[11	CPTN2A[10	DCPTN2A[9]	DCPTN2A[8]	DCPTN2A[7]	DCPTN2A[6]	DCPTN2A[5]	DCPTN2A[4]	DCPTN2A[3]	DCPTN2A[2]	DCPTN2A[1]	DCPTN2A[0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN2A	0	R/W	DCLK pattern (DCPTA47-DCPTA32)auxiliary The specified bit pattern is output in resolution of ENC clock units

5.9.34 DCLKPTN3A

DCLK Auxiliary Pattern 3 Register

DCLKPTN3A 0003:0842 offset: 0x42 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCPTN3A[15]	DCPTN3A[14]	DCPTN3A[13]	DCPTN3A[12]	DCPTN3A[11]	DCPTN3A[10]	DCPTN3A[9]	DCPTN3A[8]	DCPTN3A[7]	DCPTN3A[6]	DCPTN3A[5]	DCPTN3A[4]	DCPTN3A[3]	DCPTN3A[2]	DCPTN3A[1]	DCPTN3A[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	DCPTN3A	0	R/W	DCLK pattern (DCPTA63-DCPTA48)auxiliary The specified bit pattern is output in resolution of ENC clock units

5.9.35 DCLKHS

Horizontal DCLK Mask Start Position

DCLKHS 0003:0844 offset: 0x44 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	DCHS[12]	DCHS[11]	DCHS[10]	DCHS[9]	DCHS[8]	DCHS[7]	DCHS[6]	DCHS[5]	DCHS[4]	DCHS[3]	DCHS[2]	DCHS[1]	DCHS[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	DCHS	0	R/W	Horizontal DCLK mask start position This is specified in number of ENC clocks from start of the horizontal sync signal

5.9.36 DCLKHSA

Horizontal auzilliary DCLK Mask Start Position

DCLKHSA 0003:0846 offset: 0x46 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	DCHSA[12]	DCHSA[11]	DCHSA[10]	DCHSA[9]	DCHSA[8]	DCHSA[7]	DCHSA[6]	DCHSA[5]	DCHSA[4]	DCHSA[3]	DCHSA[2]	DCHSA[1]	DCHSA[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	DCHSA	0	R/W	Horizontal DCLK (auxiliary) mask start position This is specified in number of ENC clocks from start of the horizontal sync signal

5.9.37 DCLKHR

Horizontal DCLK Mask Start Range

DCLKHR 0003:0848 offset: 0x48 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	DCHR[12]	DCHR[11]	DCHR[10]	DCHR[9]	DCHR[8]	DCHR[7]	DCHR[6]	DCHR[5]	DCHR[4]	DCHR[3]	DCHR[2]	DCHR[1]	DCHR[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	DCHR	0	R/W	Horizontal DCLK mask range This is specified in ENC clocks

5.9.38 DCLKVS

Vertical Mask start position

DCLKVS 0003:084A offset: 0x4A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	DCVS[12]	DCVS[11]	DCVS[10]	DCVS[9]	DCVS[8]	DCVS[7]	DCVS[6]	DCVS[5]	DCVS[4]	DCVS[3]	DCVS[2]	DCVS[1]	DCVS[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	DCVS	0	R/W	DCLK vertical mask start position This is specified in lines from vertical sync signal

5.9.39 DCLKVR

Vertical DCLK Mask Start Range

DCLKVR 0003:084C offset: 0x4C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	DCVR[12]	DCVR[11]	DCVR[10]	DCVR[9]	DCVR[8]	DCVR[7]	DCVR[6]	DCVR[5]	DCVR[4]	DCVR[3]	DCVR[2]	DCVR[1]	DCVR[0]
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12:0	DCVR	0	R/W	DCLK vertical mask range This is specified in number of lines

5.9.40 CAPCTL

Closed caption control register

CAPCTL 0003:084E offset: 0x4E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	CADF[6]	CADF[5]	CADF[4]	CADF[3]	CADF[2]	CADF[1]	CADF[0]	RSV	RSV	RSV	RSV	RSV	RSV	CAPF[1]	CAPF[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-	-	-	-	-	R/W	R/W
Default	-	0	0	0	0	0	0	0	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	CADF	0	R/W	Closed caption default data register
7:2	RSV			Reserved
1:0	CAPF	0	R/W	Closed caption field select, Specify the fields on which closed captioning is enabled » 0: No data output « » 1: Even field « » 2: Odd field « » 3: Both fields «

5.9.41 CAPDO

Closed caption odd field data

CAPDO 0003:0850 offset: 0x50 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	CADO0[6]	CADO0[5]	CADO0[4]	CADO0[3]	CADO0[2]	CADO0[1]	CADO0[0]	RSV	CADO1[6]	CADO1[5]	CADO1[4]	CADO1[3]	CADO1[2]	CADO1[1]	CADO1[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	CADO0	0	R/W	Closed caption data odd field (CADO06-CADO00) Specify the ASCII code for the 1st byte to be transmitted in odd field
7	RSV			Reserved
6:0	CADO1	0	R/W	Closed caption data odd field (CADO16-CADO10) Specify the ASCII code for the 2nd byte to be transmitted in odd field

5.9.42 CAPDE

Closed caption even field data

CAPDE 0003:0852 offset: 0x52 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	CADE0[6]	CADE0[5]	CADE0[4]	CADE0[3]	CADE0[2]	CADE0[1]	CADE0[0]	RSV	CADE1[6]	CADE1[5]	CADE1[4]	CADE1[3]	CADE1[2]	CADE1[1]	CADE1[0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15	RSV			Reserved
14:8	CADE0	0	R/W	Closed caption data even field (CADE06-CADE00) Specify the ASCII code for the 1st byte to be transmitted in even field
7	RSV			Reserved
6:0	CADE1	0	R/W	Closed caption data even field (CADE16-CADE10) Specify the ASCII code for the 2nd byte to be transmitted in even field

5.9.43 ATR0

Video Attribute Data #0

ATR0 0003:0854 offset: 0x54 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ATR0[7]	ATR0[6]	ATR0[5]	ATR0[4]	ATR0[3]	ATR0[2]	ATR0[1]	ATR0[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	ATR0	0	R/W	Video attribute data register 0 (ATR07-ATR00) NTSC - Set the WORD0 data. Bit5-3 is WORD0-B, Bit2-0 is WORD0-A

5.9.44 ATR1

Video Attribute Data #1

ATR1 0003:0856 offset: 0x56 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ATR1[7]	ATR1[6]	ATR1[5]	ATR1[4]	ATR1[3]	ATR1[2]	ATR1[1]	ATR1[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	ATR1	0	R/W	Video attribute data register 1 (ATR17-ATR10) NTSC - Set the WORD1 and WORD2 data. Bit7-4 is WORD2, Bit3-0 is WORD1 PAL - Set the GROUP1 and GROUP2 data. Bit7-4 is GROUP2, Bit3-0 is GROUP1

5.9.45 ATR2

Video Attribute Data #2

ATR2 0003:0858 offset: 0x58 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ATR2[7]	ATR2[6]	ATR2[5]	ATR2[4]	ATR2[3]	ATR2[2]	ATR2[1]	ATR2[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	ATR2	0	R/W	Video attribute data register 2 (ATR27-ATR20) NTSC - Set CRC data and enable attribute insertion. Bit7 is ATR_EN, Bit6 is unused, Bit5-0 is CRC PAL - Set GROUP3 and GROU4 data and enable attribute insertion. Bit7 is ATR_EN, Bit6 is ununsed, Bit5-3 is GROUP4 and Bit2-9 is GROUP3 ATR_EN: Attribute data insertion enable 0: No insertion 1: Insertion

5.9.46 EPSON_LCDCTL

EPSON LCD Control Register

EPSON_LCDCTL 0003:085A offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	YSCLS	XINHS	XINHL	SYSFID	SYSSE	GCPS[2]	GCPS[1]	GCPS[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7	YSCLS	0	R/W	Low pulse number of YSCL » 0: one pulse (1/2 reset drive) « » 1: two pulses (1/2 select drive) «
6	XINHS	0	R/W	XINH Signal select » 0: DC output « » 1: TG controlled «
5	XINHL	0	R/W	XINH DC level » 0: L level output « » 1: H level output «
4	SYSFID	0	R/W	SYS function applied field ID select
3	SYSSE	0	R/W	SYS function enable » 0: Off « » 1: On « Note: setting '1 resets the vertical counter one line earlier in the field selected by SYSFID
2:0	GCPS	0	R/W	GCP pattern select » 0: ROM (Type 0) « » 1: ROM (Type 1) « » 2: ROM (Type 2) « » 3: ROM (Type 3) « » 4: RAM « » 5-7: Reserved « Note: When RAM is used, data written in RAM address 0-63 is shifted out by one bit from MSB to LSB and output as GCP pulse

5.9.47 CASIO_LCDCTL

CASIO LCD Control Register

CASIO_LCDCTL 0003:085A offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	CRIT	CSTB	CGRES	CDM
R/W	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:4	RSV			Reserved
3	CRIT	0	R/W	RIT port control » 0: L level output « » 1: H level output « Note: Setting is enabled at the rising edge of horizontal sync signal
2	CSTB	0	R/W	STBYB port control » 0: L level output « » 1: H level output « Note: CP output is fixed at H level when 0
1	CGRES	0	R/W	GRES port control » 0: Normal « » 1: Fixed L level «
0	CDM	0	R/W	Display mode » 0: Normal « » 1: Vertical reverse mode«

5.9.48 UDISP_LCDCTL

UDISP LCD Control Register

UDISP_LCDCTL 0003:085A offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	FSW[7]	FSW[6]	FSW[5]	FSW[4]	FSW[3]	FSW[2]	FSW[1]	FSW[0]
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	RSV			Reserved
7:0	FSW	0	R/W	Frame start pulse width This is Specified in ENC clocks

5.9.49 STN_LCDCTL

STN LCD Control Register SCPROG – Sub-carrier programming Register

STN_LCDCTL 0003:085A offset: 0x5A default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	SDW[1]	SDW[0]
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Reset Value	R/W	Function
15:2	RSV			Reserved
1:0	SDW	0	R/W	STN-LCD data bus width » 0: 8 bits « » 1: 4 bits « » 2: 12 bits « » 3: Reserved «

5.9.50 VSTAT

Video Status Register

VSTAT 0003:085C offset: 0x5C default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	CAEST	CAOST	RSV	RSV	RSV	FIDST	VSST	HSST	UDBAL	UDFUL
R/W	-	-	-	-	-	-	R	R	-	-	-	R	R	R	R	R
Default	-	-	-	-	-	-	0	0	-	-	-	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:10	RSV			Reserved
9	CAEST	0	R	Closed caption status (even field) » 0: Ready « » 1: Data is being input « Note: The bit automatically becomes '0', when transmission is done
8	CAOST	0	R	Closed caption status (odd field). » 0: Ready « » 1: Data is being input « Note: The bit automatically becomes '0', when transmission is done
7:5	RSV			Reserved
4	FIDST	0	R	Field ID monitor
3	VSST	0	R	VSYNC monitor
2	HSST	0	R	HSYNC monitor
1	UDBAL	0	R	uDisplay 'Balance' signal monitor
0	UDFUL	0	R	uDisplay 'Full' signal monitor

5.9.51 RAMADR

GCP / FRP RAM table address

RAMADR 0003:085E offset: 0x5E default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RAMADR[5]	RAMADR[4]	RAMADR[3]	RAMADR[2]	RAMADR[1]	RAMADR[0]
R/W	-	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:6	RSV			Reserved
5:0	RAMADR	0	R/W	GCP/FRC table RAM address. Note: Auto-increment is done after evey access to RAMPORT register, When RAMADDR = 0x3F, auto-increment does not happen

5.9.52 RAMPORT

GCP / FRP RAM Data Port

RAMPORT 0003:0860 offset: 0x60 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AMPORT[1	AMPORT[1	AMPORT[1	AMPORT[1	AMPORT[1	AMPORT[1	RAMPORT[9	RAMPORT[8	AMPORT[7	AMPORT[6	AMPORT[5	AMPORT[4	AMPORT[3	AMPORT[2	AMPORT[1	AMPORT[0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:0	RAMPORT	0	R/W	RAM data port At reading, the data in the address specified in the RAMA register can be read. At writing, the data is written to the address specified in the RAMA register. The RAMA is automatically incremented every access to the RAMP register in both write and read cases

5.9.53 DACTST

DAC Test Register

DACTST 0003:0862 offset: 0x62 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	RSV	DACOE	DACDC	DALVL[9]	DALVL[8]	DALVL[7]	DALVL[6]	DALVL[5]	DALVL[4]	DALVL[3]	DALVL[2]	DALVL[1]	DALVL[0]
R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:12	RSV			Reserved
11	DACOE	0	R/W	DAC cell OE control » 0: Normal « » 1: DAOUT L level output«
10	DACDC	0	R/W	DAC DC output mode » 0: Normal « » 1: DC output mode « Note: Setting “1” converts the value written in the DALVL register to DAC and directly outputs from DAOUT
9:0	DALVL	0	R/W	DC level control

5.9.54 YCOLVL

YOUT / COUT level Register

YCOLVL 0003:0864 offset: 0x64 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YLVL[7]	YLVL[6]	YLVL[5]	YLVL[4]	YLVL[3]	YLVL[2]	YLVL[1]	YLVL[0]	CLVL[7]	CLVL[6]	CLVL[5]	CLVL[4]	CLVL[3]	CLVL[2]	CLVL[1]	CLVL[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:8	YLVL	0	R/W	YOUT DC level Specify the DC output level from YOUT pins when YOUT/COUT pin DC output mode (YCDC=1)
7:0	CLVL	0	R/W	COUT DC level. Specify the DC output level from COUT pins when YOUT/COUT pin DC output mode (YCDC=1)

5.9.55 SCPROG

Sub-carrier programming Register

SCPROG 0003:0866 offset: 0x66 default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSV	RSV	RSV	SCPRG	RSV	RSV	SCSD[9]	SCSD[8]	SCSD[7]	SCSD[6]	SCSD[5]	SCSD[4]	SCSD[3]	SCSD[2]	SCSD[1]	SCSD[0]
R/W	-	-	-	R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Reset Value	R/W	Function
15:13	RSV			Reserved
12	SCPRG	0	R/W	Sub-carrier phase program mode. When 1, the initial phase degree of sub-carrier can be programmed to the specified value in SCSD register. The sub-carrier phase is immediately updated when CPU writes this register. When 0, internal preset value is used for sub-carrier phase » 0: Fixed by Hardware « » 1: Program mode «
11:10	RSV			Reserved
9:0	SCSD	0	R/W	Sub-carrier initial phase value The degree can be specified by SCSD/1024*360.