



BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

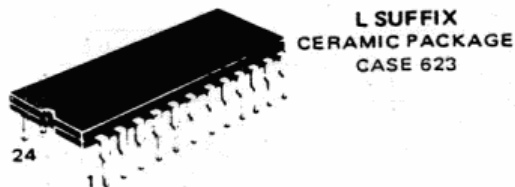
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc ($\pm 5\%$) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input

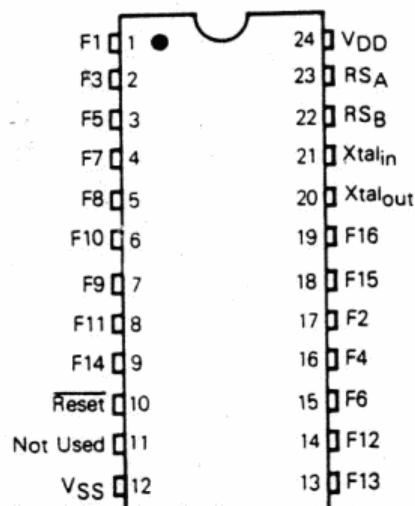
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR



PIN ASSIGNMENT



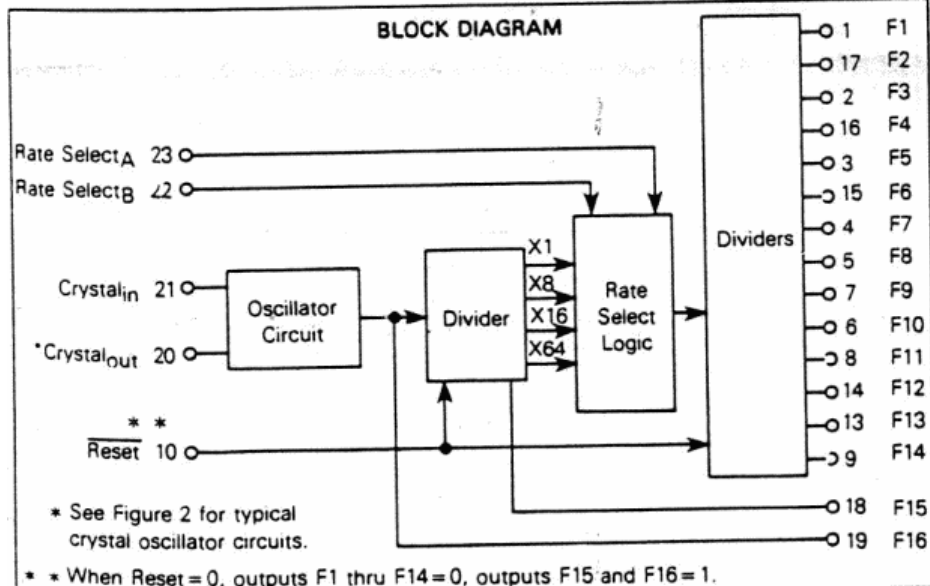
V_{DD} = Pin 24
 V_{SS} = Pin 12

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9386R2

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits.

** When Reset = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	- 40°C		25°C			+ 85°C		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Supply Voltage	V _{DD}	—	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V	
Output Voltage	V _{out}	"0" Level	5.0	—	0.05	—	0	0.05	—	0.05	V
		"1" Level	5.0	4.95	—	4.95	5.0	—	4.95	—	V
Input Voltage (V _O = 4.5 or 0.5 V)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V	
Output Drive Current (V _{OH} = 2.5 V) Source	I _{OH}	5.0	-0.23	—	-0.20	-1.7	—	-0.16	—	mA	
	(V _{OL} = 0.4 V) Sink	I _{OL}	5.0	0.23	—	0.20	0.78	—	0.16	—	mA
Input Current Pins 21, 22, 23	I _{in}	—	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA	
		Pin 10	5.0	—	—	-1.5	—	-7.5	—	—	μA
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	—	—	—	pF	
Quiescent Dissipation	P _Q	5.0	—	2.5	—	0.015	2.5	—	15	mW	
Power Dissipation**† (Dynamic plus Quiescent) (C _L = 15 pF)	P _D	5.0	P _D = (7.5 mW/MHz) f + P _Q								mW
Output Rise Time** t _r = (3.0 ns/pF) C _L + 25 ns	t _{TLH}	5.0	—	—	—	70	200	—	—	ns	
Output Fall Time** t _f = (1.5 ns/pF) C _L + 47 ns	t _{THL}	5.0	—	—	—	70	200	—	—	ns	
Input Clock Frequency	f _{CL}	5.0	—	1.85	—	—	1.85	—	1.85	MHz	
Clock Pulse Width	t _{W(C)}	—	200	—	200	—	—	200	—	ns	
Reset Pulse Width	t _{W(R)}	—	500	—	500	—	—	500	—	ns	

†For dissipation at different external capacitance (C_L) refer to corresponding formula:

$$P_T(C_L) = P_D + 2.6 \times 10^{-3}(C_L - 15 \text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

TABLE 1 — OUTPUT CLOCK RATES

Rate Select		Rate
B	A	
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz)			
	X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is buffered oscillator output.

FIGURE 1. — DYNAMIC SIGNAL WAVEFORMS

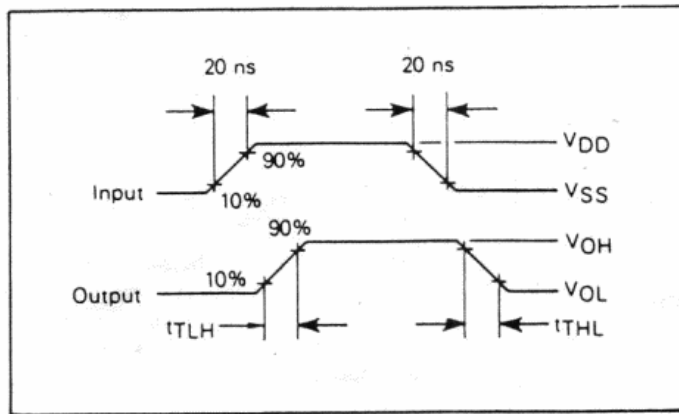
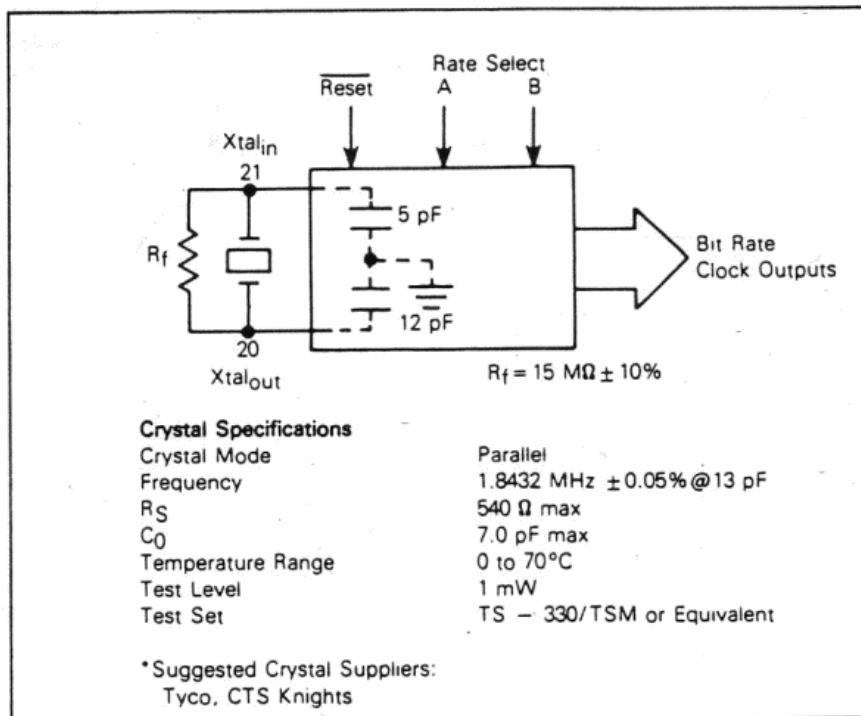


FIGURE 2 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT



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